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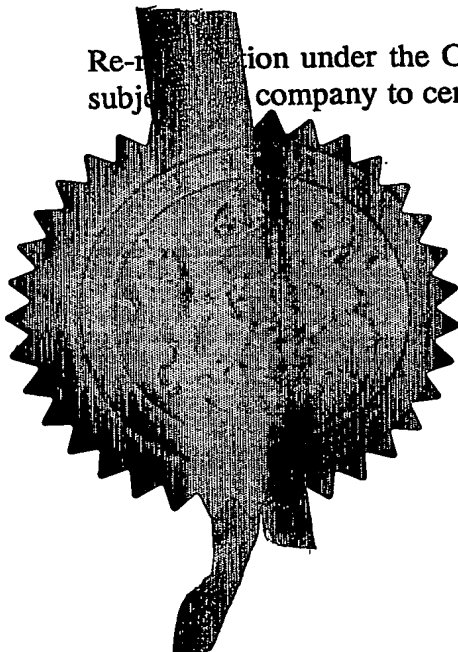
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Signed

Dated 24 November 2003



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GB 0224903.5

By virtue of a direction given under Section 30 of the Patents Act 1977, the application is proceeding in the name of:

GOLDPOWER LIMITED,
Sea Meadow House,
PO BOX 116,
Blackburn Highway Road,
Town Tortola,
British Virgin Islands

Incorporated in the British Virgin Islands,

[ADP No. 08752552001]

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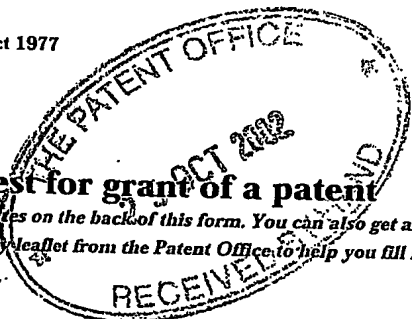
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(Rule 16)



28OCT02 E758707-5 002246
P01/7700 0.00-0224903.5

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1. Your reference

P/13675.GB JMP

2. Patent application number

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0224903.5

25 OCT 2002

3. Full name, address and postcode of the or of each applicant (underline all surnames)

SIMAGE OY
TEKNIKANTIE 14
FIN-02150 ESPOO
FINLAND

Patents ADP number (if you know it)

If the applicant is a corporate body, give the country/state of its incorporation

FINLAND

SECTION 30 (1977 ACT) APPLICATION FILED 23/10/03
7347016003

4. Title of the invention

CIRCUIT SUBSTRATE AND METHOD

5. Name of your agent (if you have one)

D Young & Co

"Address for service" in the United Kingdom to which all correspondence should be sent (including the postcode)

21 New Fetter Lane
London
EC4A 1DA

Patents ADP number (if you know it)

59006

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and (if you know it) the or each application number

Country

Priority application number
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Date of filing
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 - b) there is an inventor who is not named as an applicant, or
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Claim(s) 8

Abstract 1


Drawing(s) 15 415 



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Request for preliminary examination and search (*Patents Form 9/77*) 1 

Request for substantive examination (*Patents Form 10/77*) 1  

Any other documents
(please specify)

11. I/We request the grant of a patent on the basis of this application.

Signature  Date 25 October 2002
D Young & Co (Agents for the Applicants)

12. Name and daytime telephone number of person to contact in the United Kingdom Julian Potter 020 7353 4343

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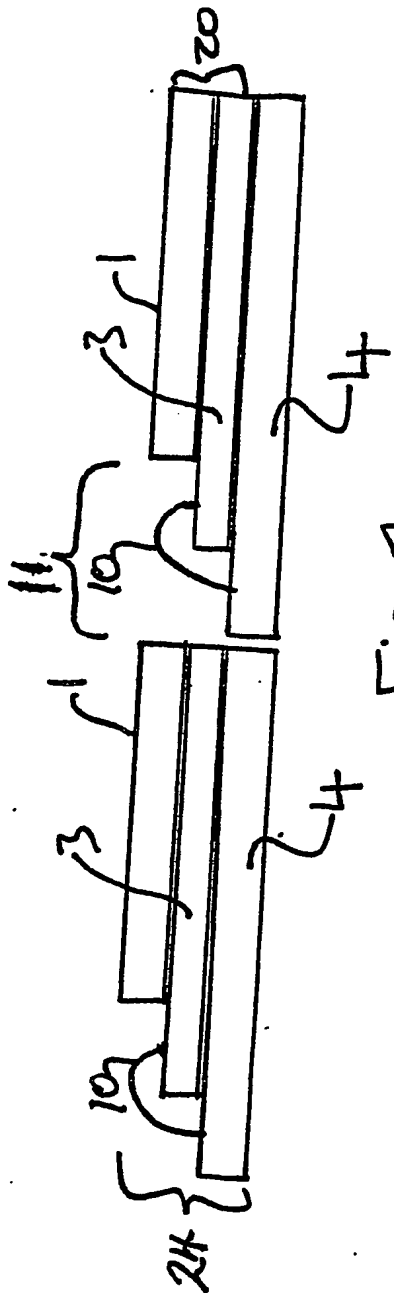


Fig. 1

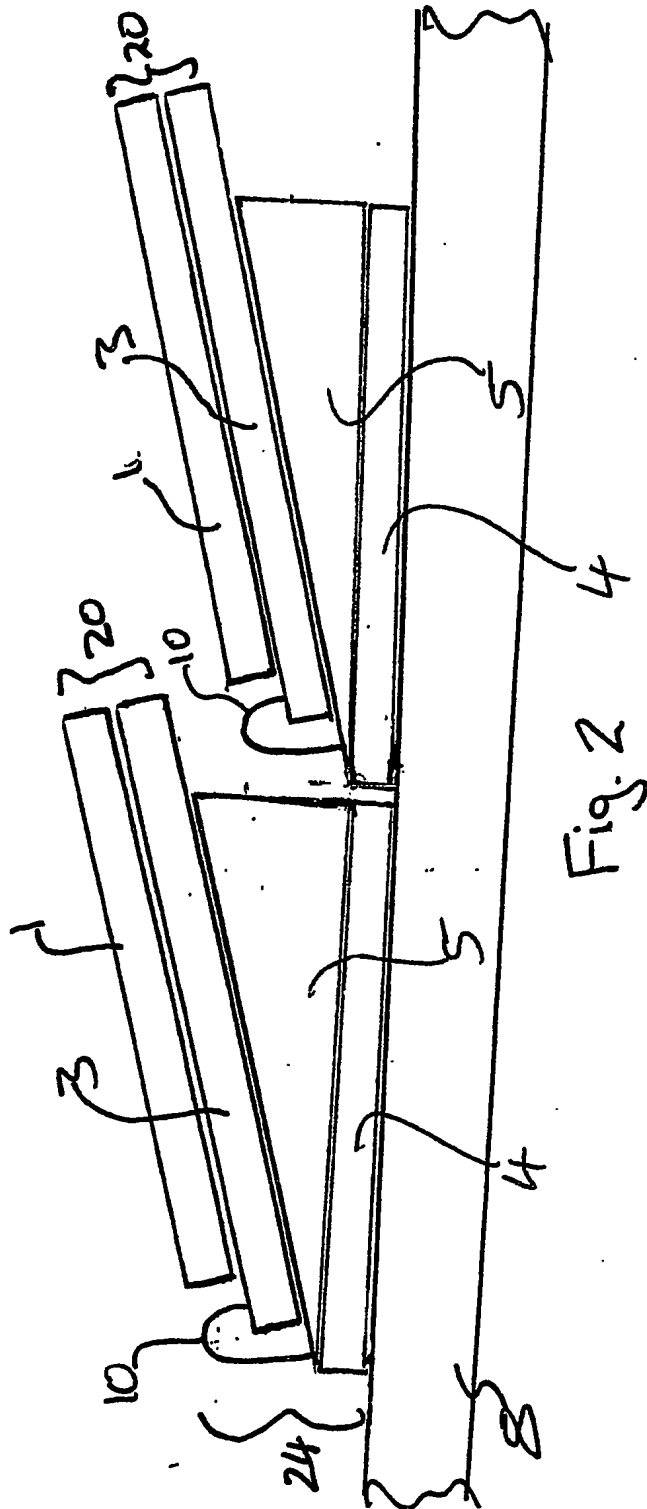


Fig. 2

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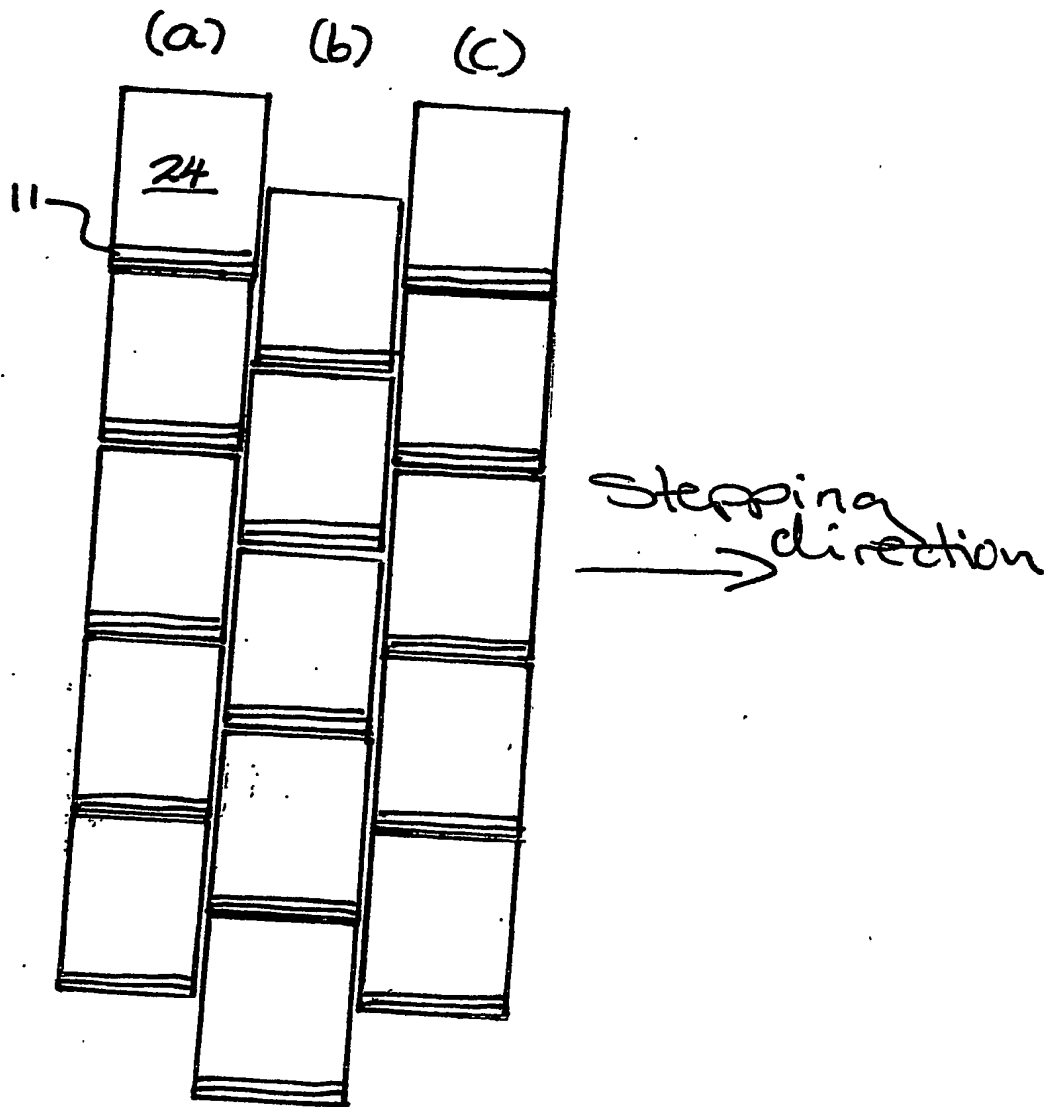


Fig. 3

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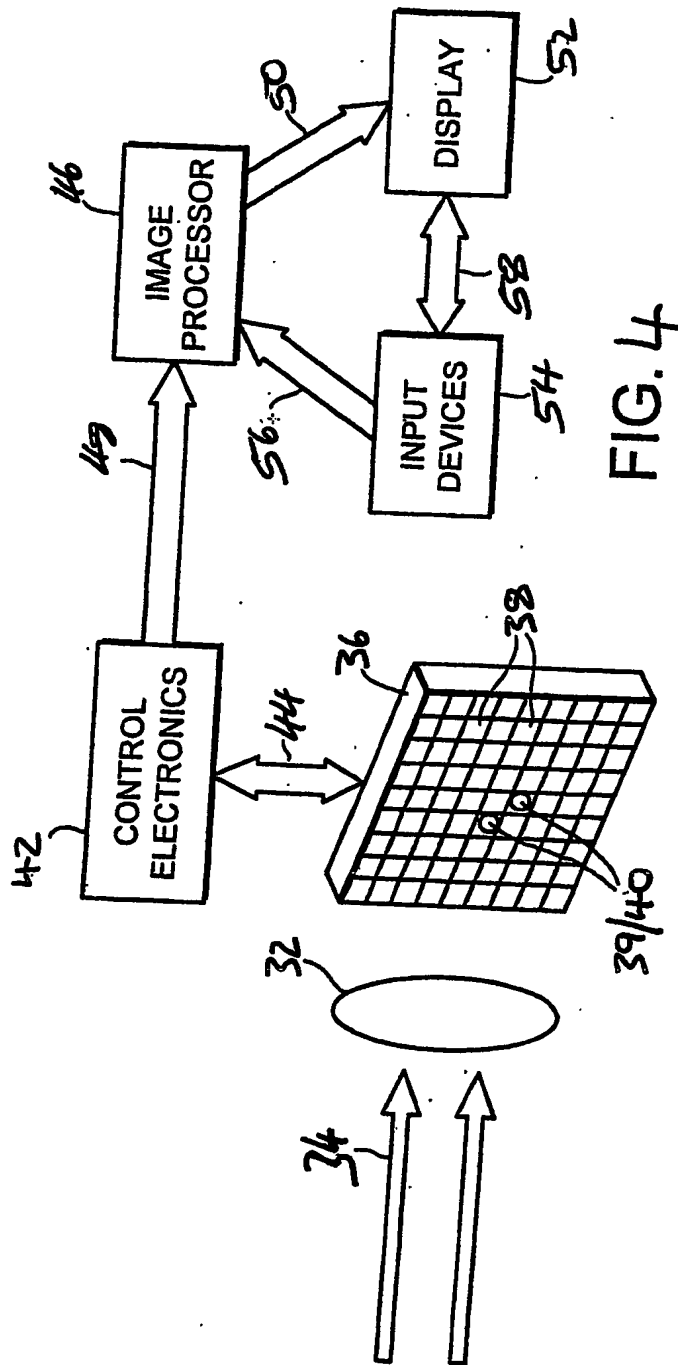


FIG. 4

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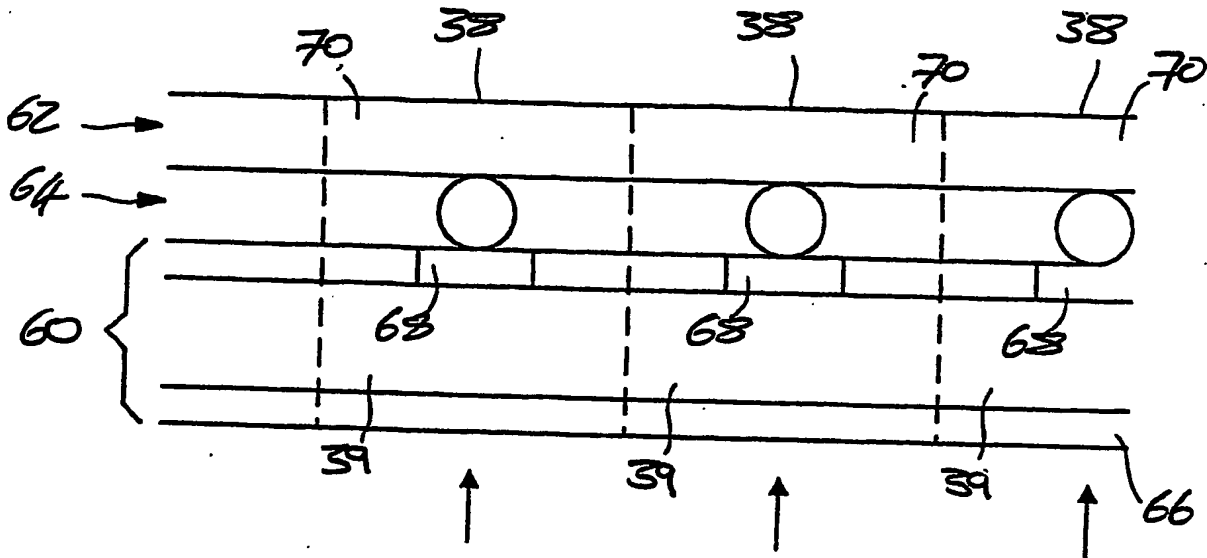
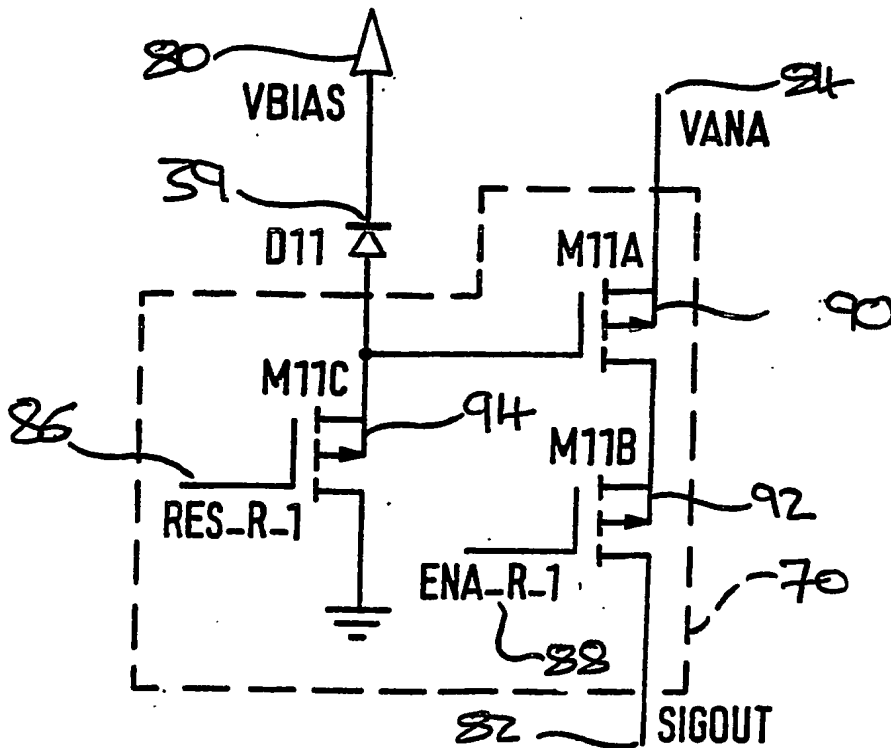


FIG. 5

FIG. 6



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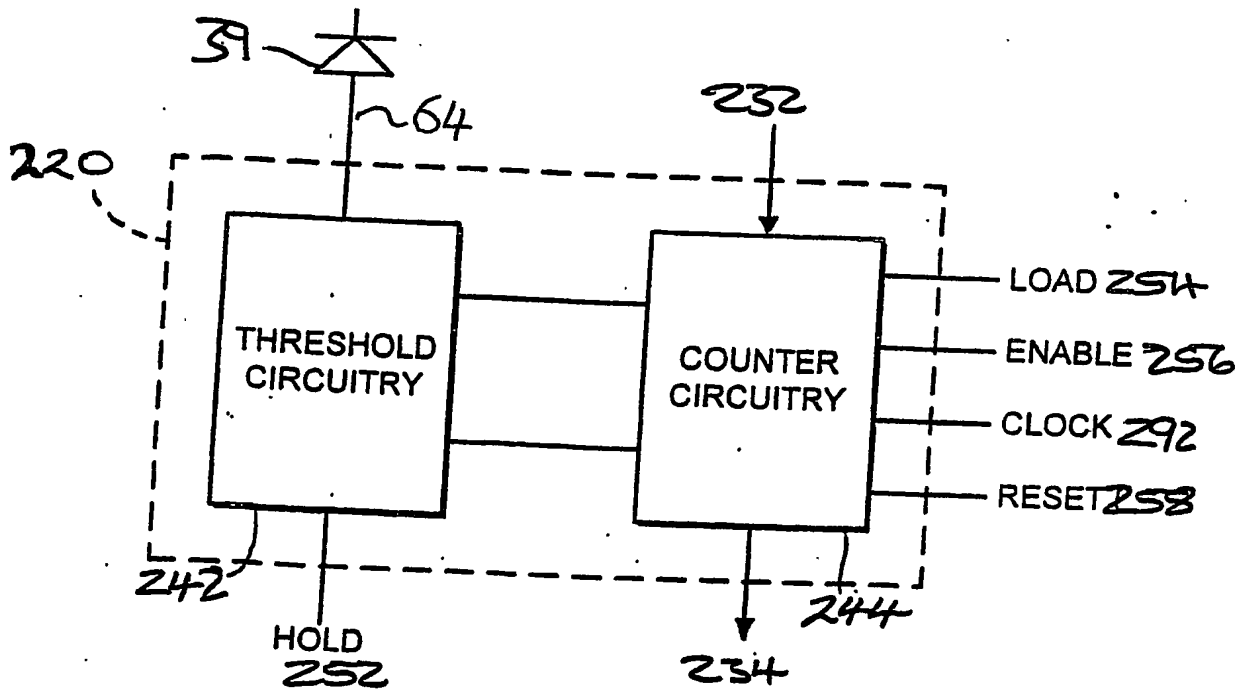
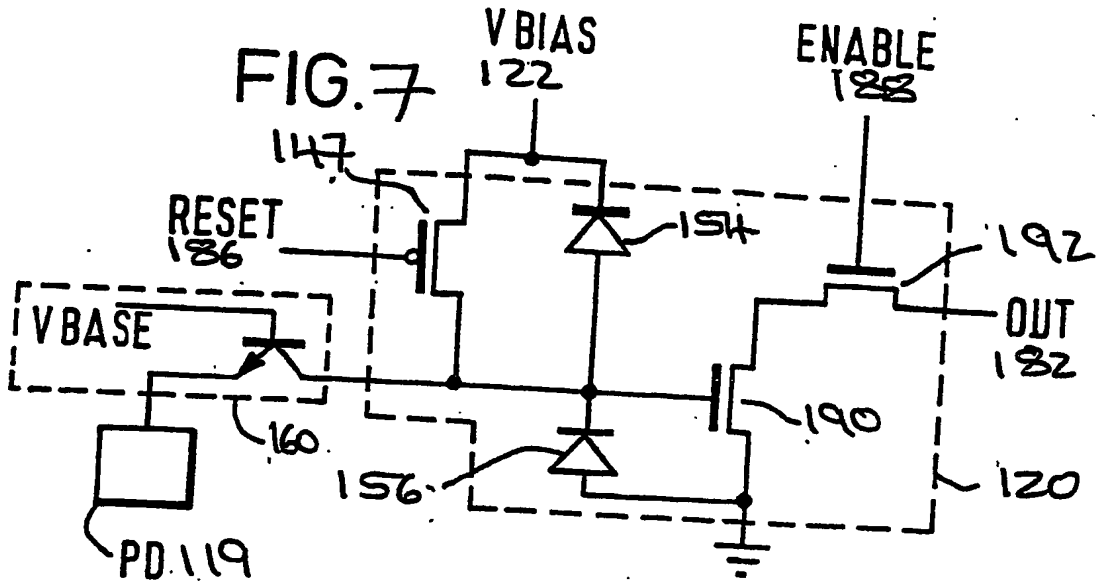


FIG. 8

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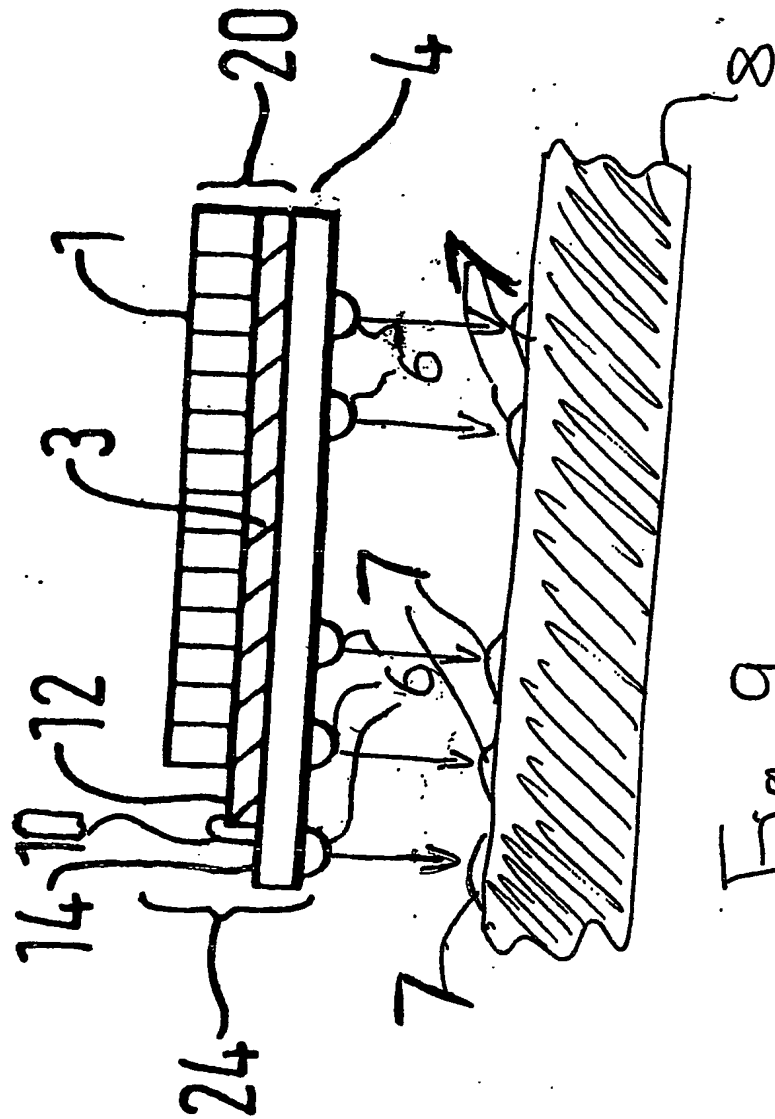


Fig. 9

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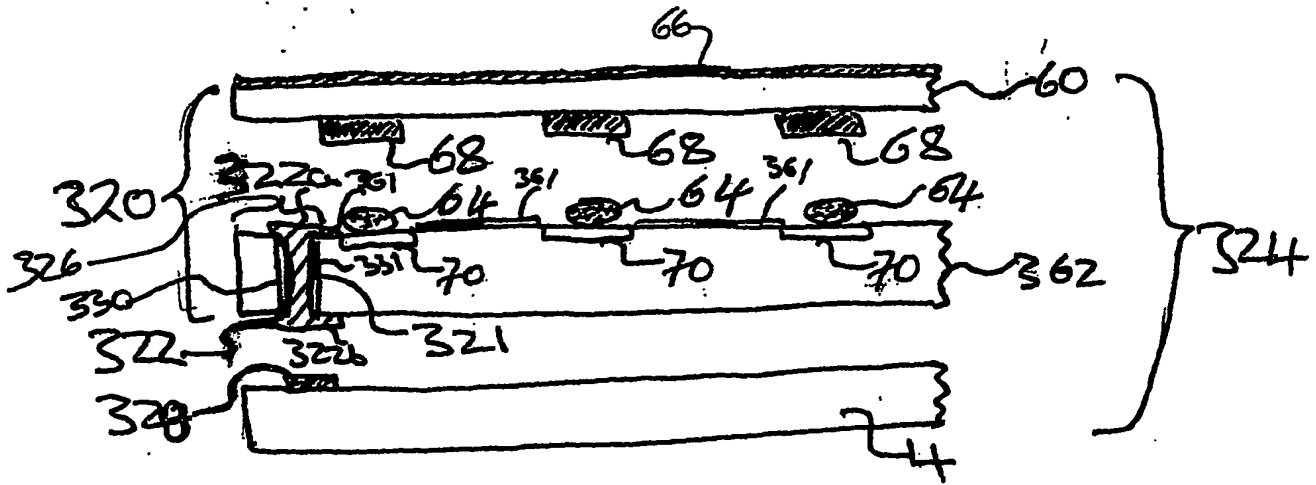


Fig. 10

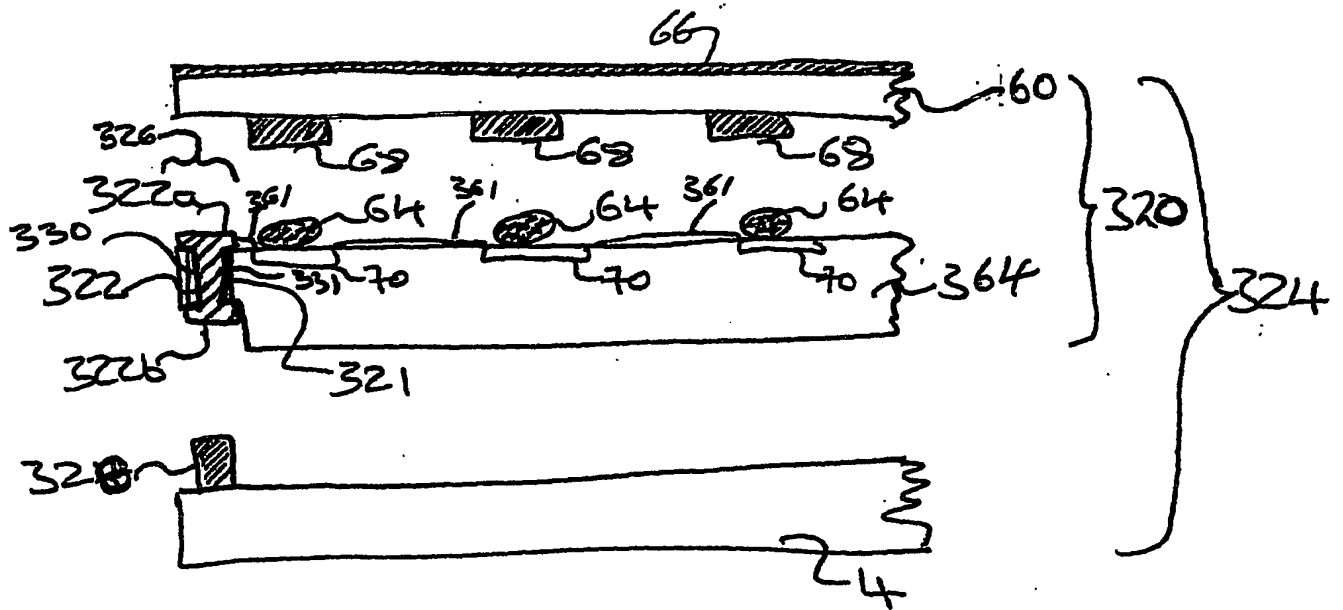


Fig. 11

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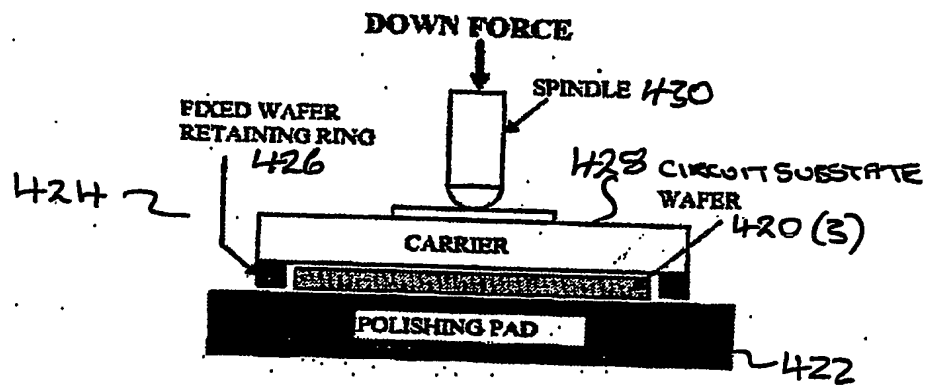


Fig. 12

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Fig. 13A

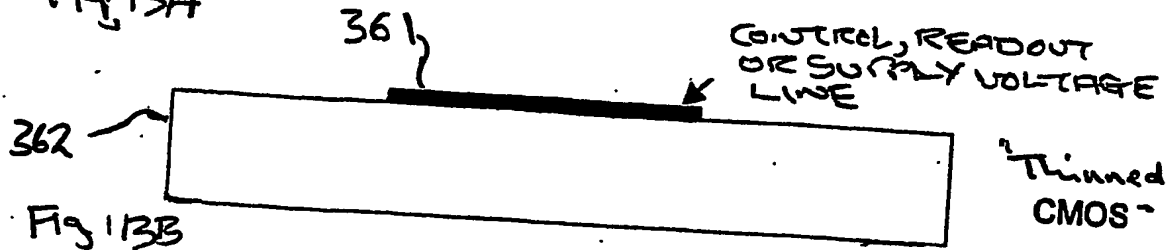


Fig. 13B

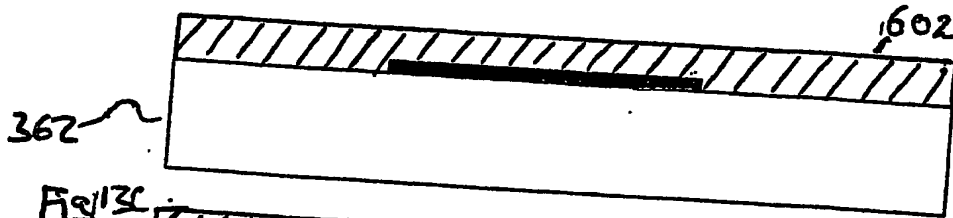


Fig. 13C

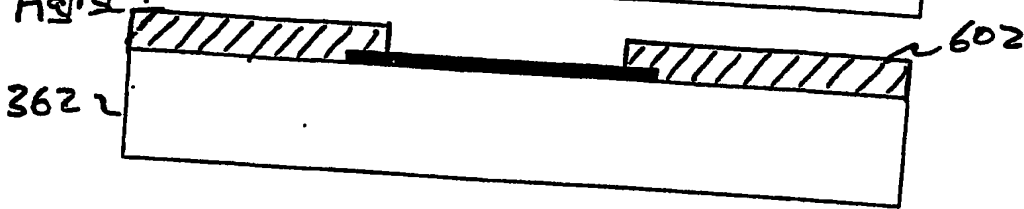


Fig. 13D

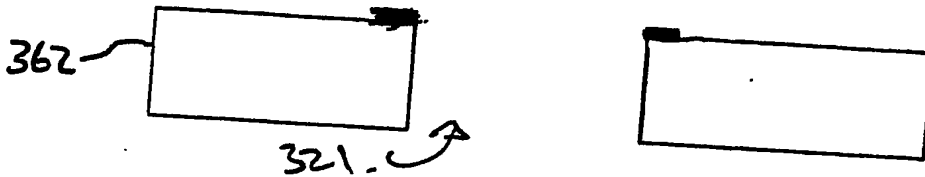


Fig. 13E

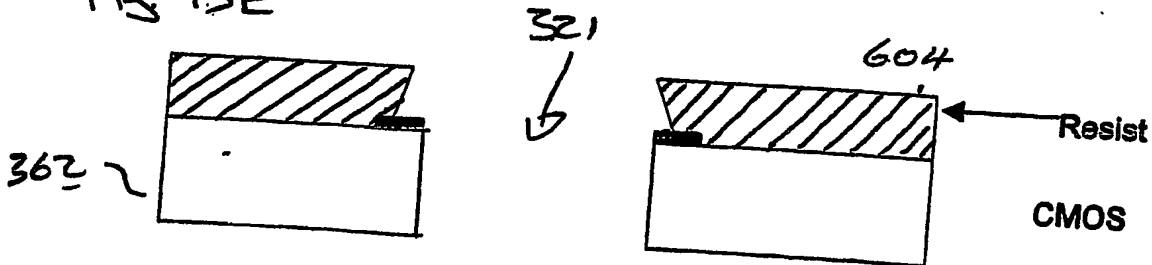


Fig. 13F

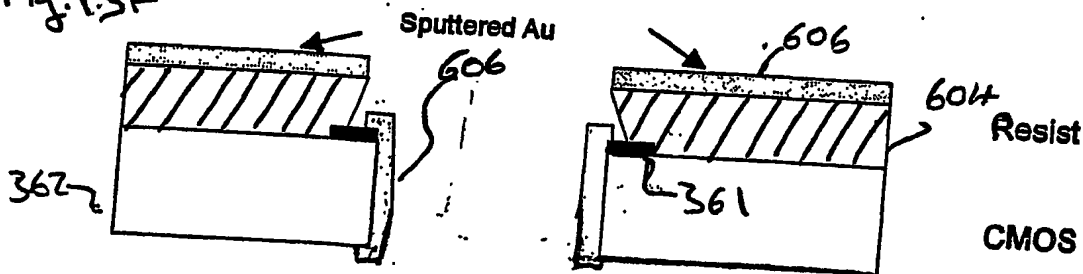
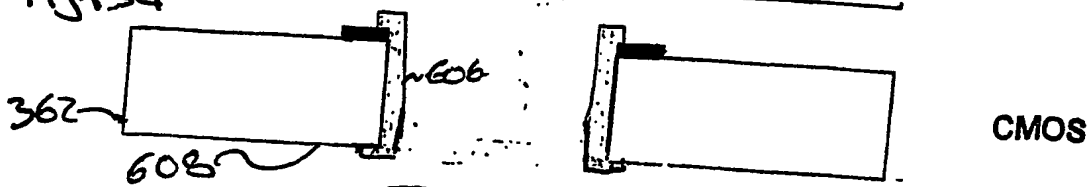


Fig. 13G



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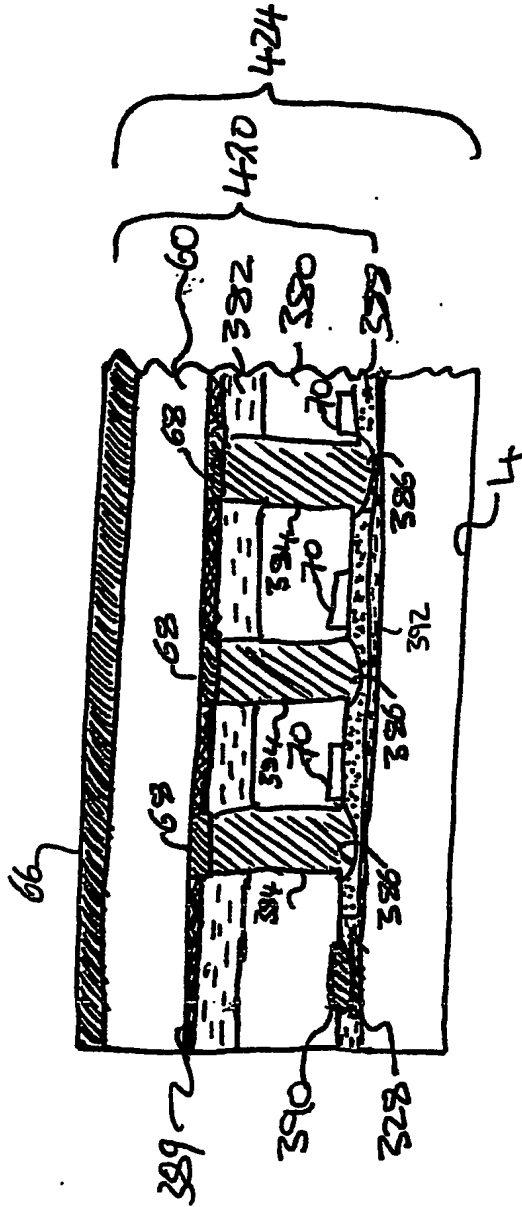


Fig. 14.

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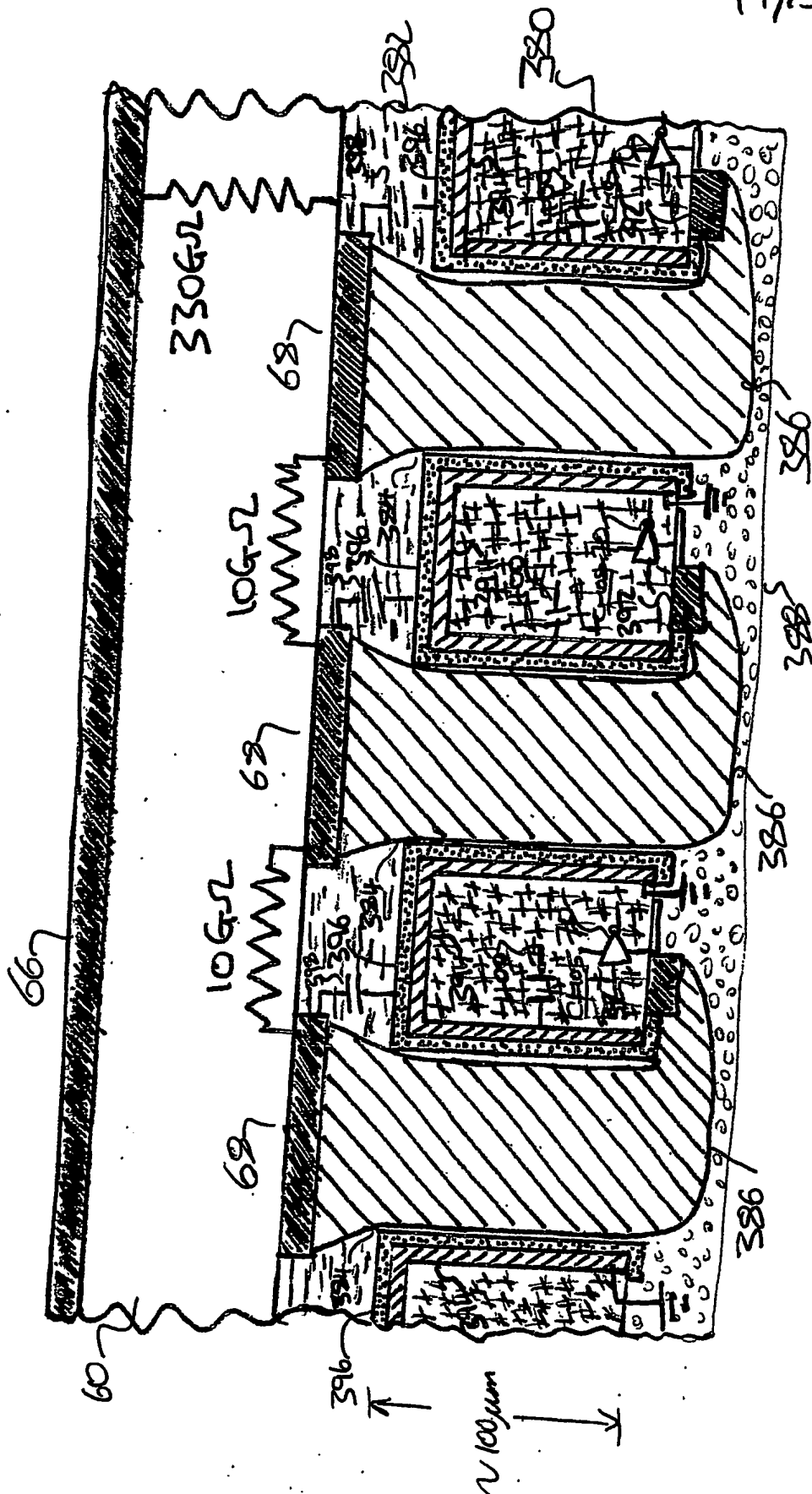
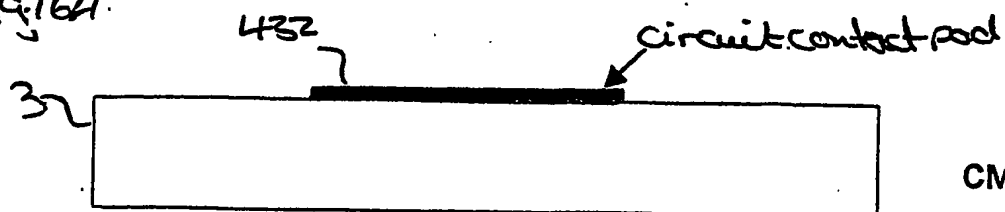


Fig. 15

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Fig 16A



CMOS

Fig 16B

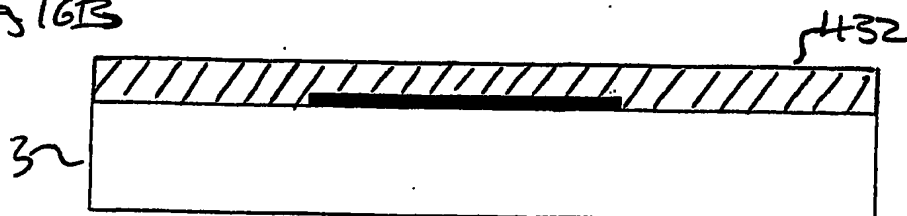


Fig 16C

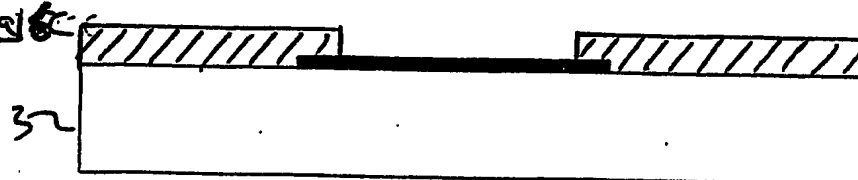


Fig 16D

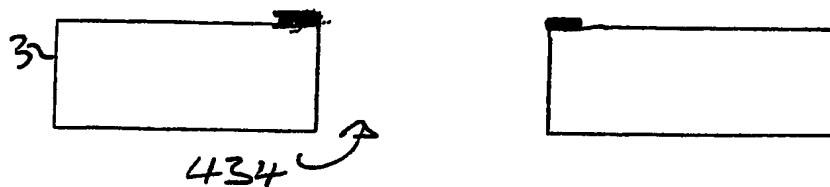


Fig 16

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Fig 16E

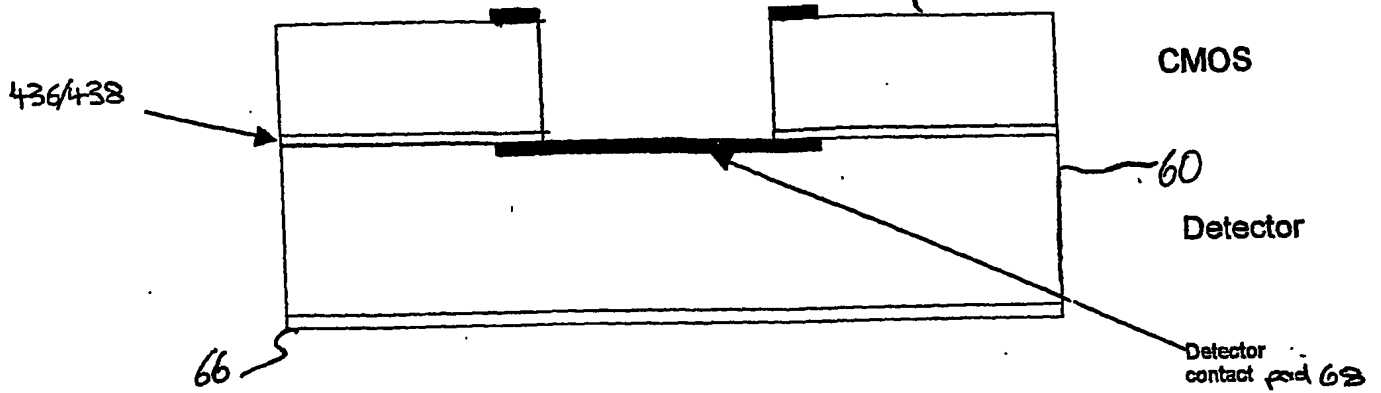


Fig 16F

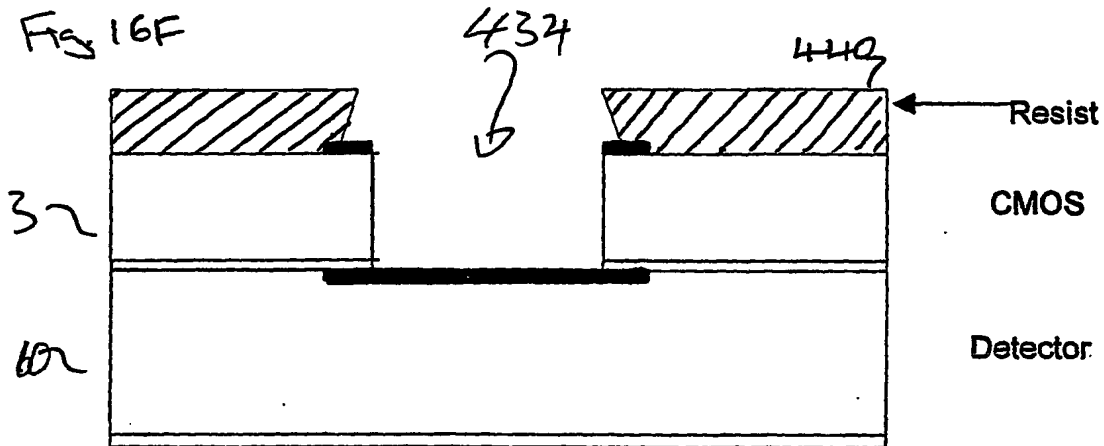


Fig 16G

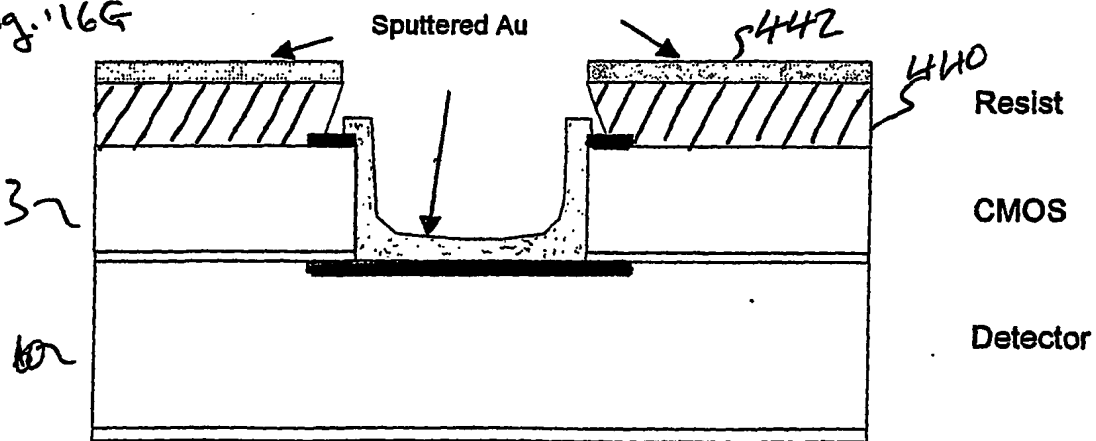


Fig 16H

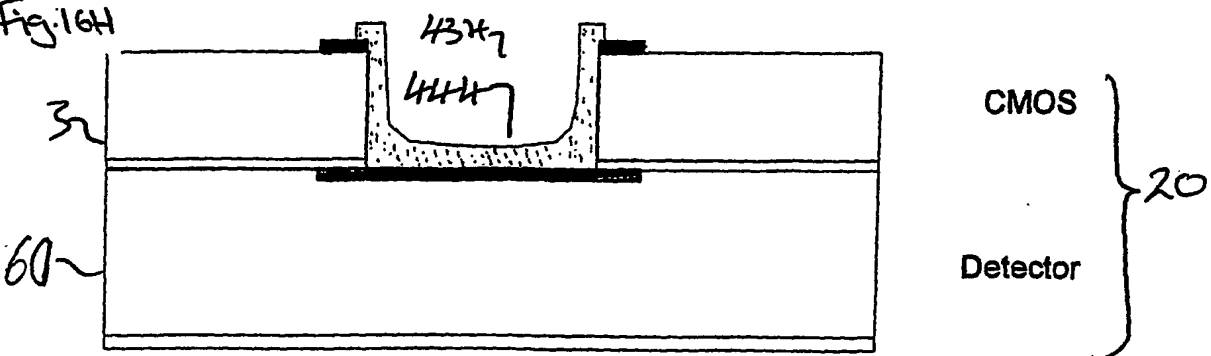


Fig. 16 (cont.)

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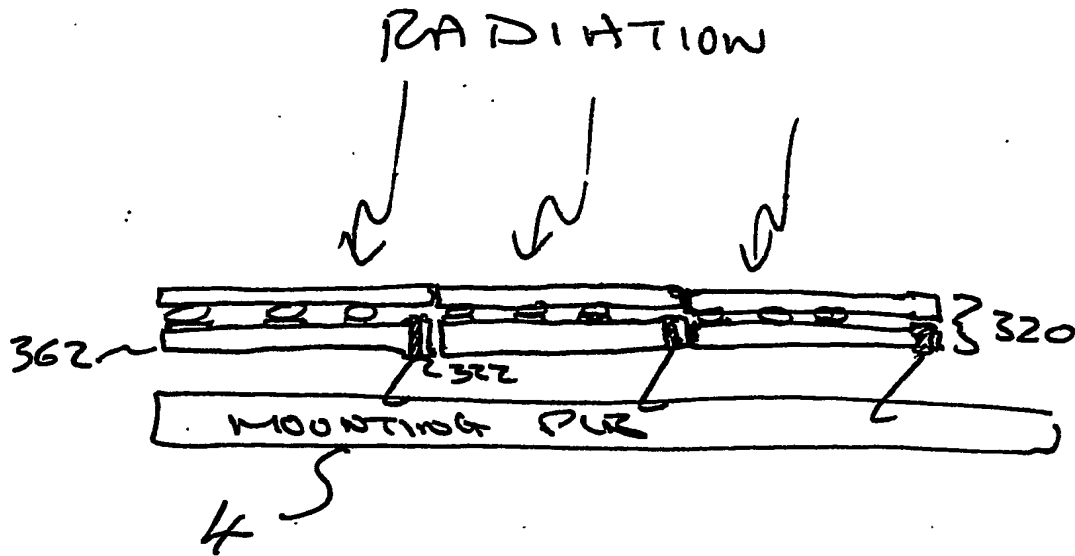


Fig. 17.

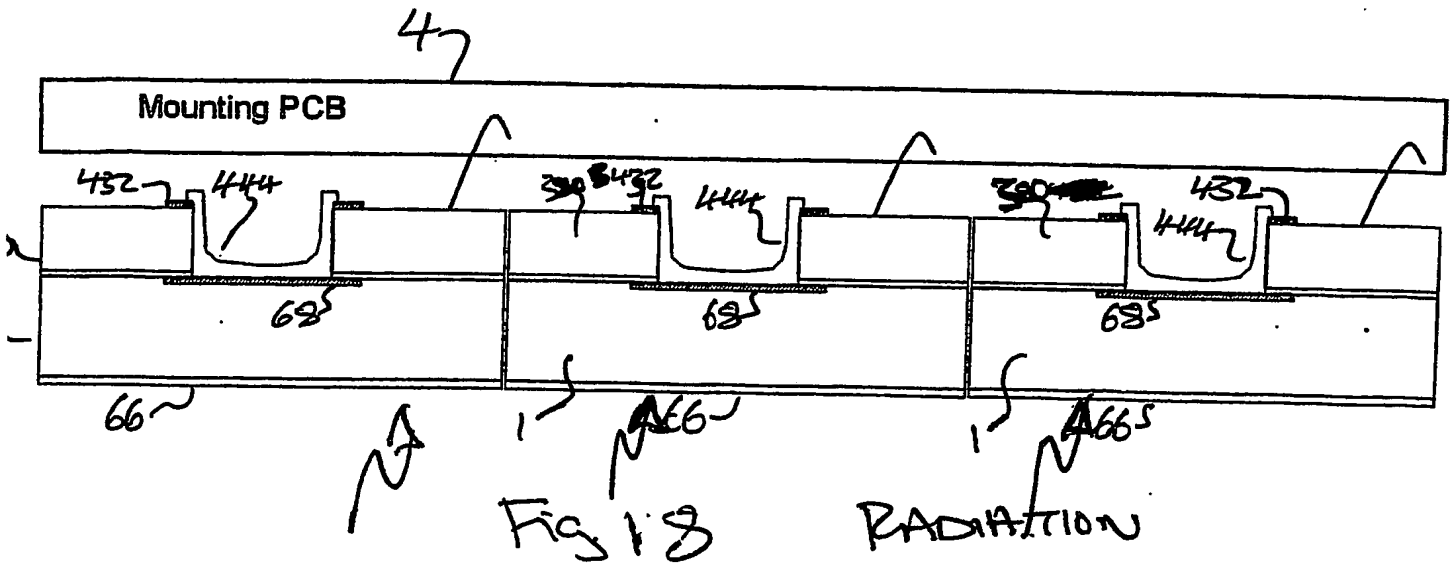


Fig. 18

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Fig 19

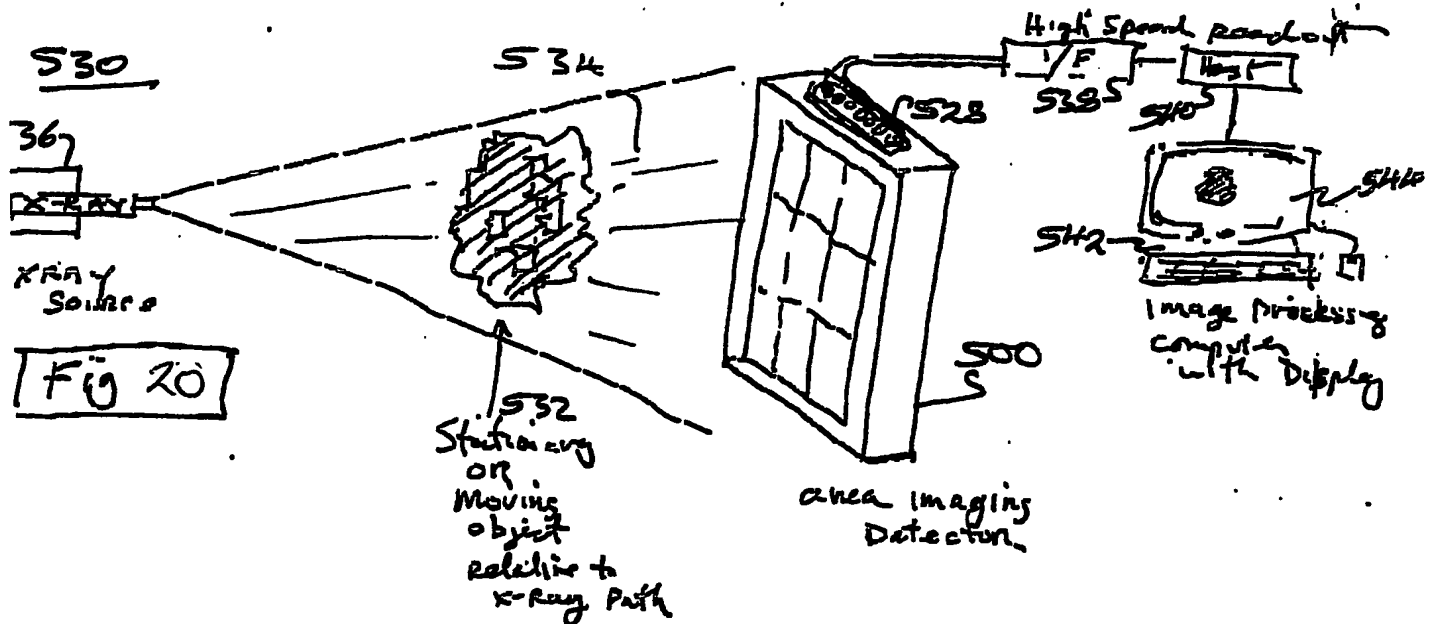
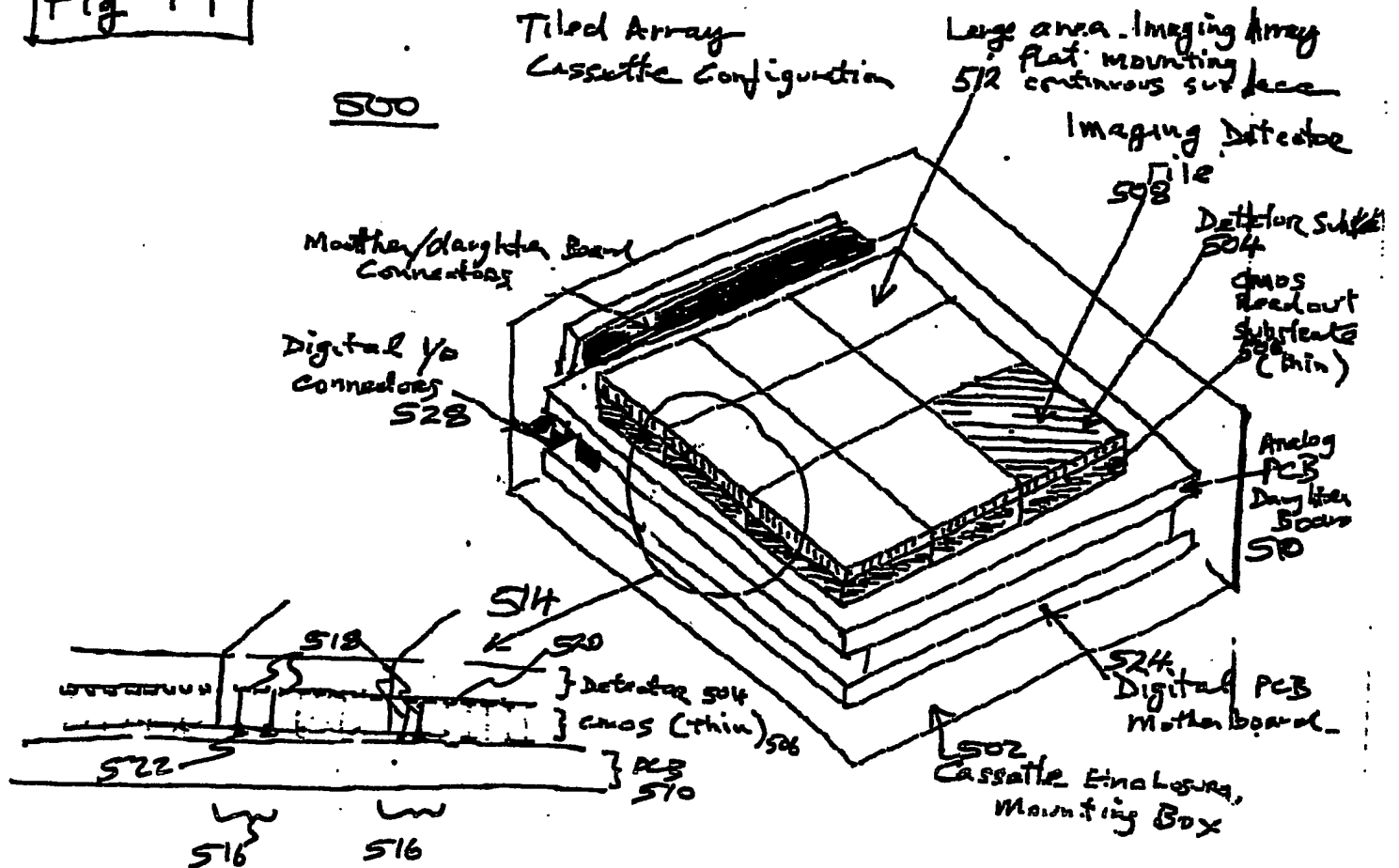


Fig 20

CIRCUIT SUBSTRATE AND METHOD

This invention relates to a circuit substrate. In particular, but not exclusively, to a circuit substrate for an imaging device for imaging radiation, the imaging device comprising an array of image cells.

5

Imaging devices comprising an array of image cells of various types are known.

Charged coupled image sensors (also known as charged coupled devices (CCDs)) form one type of known imaging device. A CCD type device operates in the following way.

1. Charge is accumulated within a depletion region created by an applied voltage. For each pixel (image cell) the depletion region has a potential well shape and constrains electrons under an electrode gate to remain within the semiconductor substrate.

15

2. Voltage is applied as a pulse to the electrode gates of the CCD device to clock each charge package to an adjacent pixel cell. The charge remains inside the semiconductor substrate and is clocked through, pixel by pixel, to a common output.

20

During this process, additional charge cannot be accumulated.

Another type of imaging device which is known is a semiconductor pixel detector which comprises a semiconductor substrate with electrodes which apply depletion voltage to each pixel position and define a charge collection volume. Typically, simple buffer circuits read out the electric signals when a photon is photo-absorbed or when ionising radiation crosses the depletion zone of the substrate. Accordingly pixel detectors of this type typically operate in a pulse mode, the numbers of hits being accumulated externally to the imaging device. The buffer circuits can either be on the same substrate (EP-A-0,287,197) as the charge collection volumes, or on a separate substrate (EP-A-0,571,135) that is mechanically bonded to a substrate

25

30

having the charge collection volumes in accordance with, for example, the well known bump-bonding technique.

A further type of device is described in International application W095/33332. In WO95/33332, an Active-pixel Semiconductor Imaging Device (ASID) is described. The ASID comprises an array of pixel or image cells including a semiconductor substrate having an array of pixel detectors (detector cells) and a further array of pixel circuits (detector cell circuits). The detector cells generate charge in response to incident radiation. Each cell circuit is associated with a detector cell and accumulates charge resulting from radiation incident on the detector cell. The detector cell circuits are individually addressable and comprise circuitry which enables charge to be accumulated from a plurality of successive radiation hits on an associated detector cell. Optionally, charge may be read out directly or individual radiation photon hits may be counted by incorporating suitable counter circuitry in the cell circuits. At a determined time, the charge or count can be read out from the cell circuit and used to generate an image based on the analogue charge or count values read from each of the cell circuits. The term "read out circuit" may also be used herein to refer to a detector cell circuit.

An example of an ASID is illustrated in Figure 1. A detector layer 1 having a large number of detector cells formed in it is mounted on a circuit layer 3. The circuit layer 3 comprises a circuit chip and is formed of a semiconductor substrate having detector cell circuits corresponding to the detector cells formed in detector layer 1.

Circuit chip 3 and detector layer 1 form an imaging device 20.

The circuit chip 3 is coupled to a mount 4 and to which external interface bond wires 10 from circuit chip 3 are coupled. The bond wires 10 take signals collected from detector layer 1 by circuit chip 3 and route them to connections on mount 4. Imaging device 20 and mount 4 form imaging device tile 24.

Typically, the imaging surface area of device 20 is of the order of one square millimetre to several square centimetres, although need not be limited to such devices

but depends on the application and semiconductor materials chosen. Therefore, if a large imaging area is required then a plurality of tiles need to be placed next to each other to form a large area imaging system.

5 However, due to the space taken up by the bond wires 10 there is "dead" imaging space 11 in between adjacent imaging device tiles 24. This "dead" space 11 results in either incomplete images being generated, or the missing data having to be compensated for, or extrapolated from the image data that was collected.

10 One way of addressing the problem of "dead" spaces between adjacent imaging tiles is disclosed in International Patent Application Publication No. WO98/03011, corresponding to U.S. Serial Number 08/899,936, incorporated herein by reference. Figure 2 schematically illustrates the arrangement disclosed in WO 98/03011. Each imaging device tile 24 includes a support 5 for the imaging device which is thus tilted
15 such that "dead" space 11 of an adjacent tile fits under the imaging device tile 24 thereby forming a substantially continuous imaging surface. A tiled array of imaging device tiles 24 are supported with edge to edge contact on a suitable support structure 8 to form a large area substantially continuous imaging surface.

20 A drawback of a tilted tile configuration is that the arrangement for tilting the tiles is relatively complex and involves more parts and components than would be necessary if the imaging devices 20 could be laid flat. Additionally, all of the imaging surface is not in the same plane which can give rise to image aberrations and artefacts. Furthermore, if support structure 8 is kept flat and substantially perpendicular to the
25 direction of incident radiation, then the radiation is incident at an angle to the imaging surface thereby inducing image aberration and artefacts, and reducing image resolution due to radiation being incident on more than one detector cell as it passes through the tilted detector layer 1.

30 Another configuration for a tiled array of imaging device tiles 24 is disclosed in International Patent Application Publication No. WO95/33332, incorporated herein by reference. WO95/33332 discloses an array of tiled imaging devices in which adjacent

columns of tiles are offset in a columnar direction, such as illustrated in Figure 3. Column (a) of device tiles 24 is offset which respect to column (b). As can be seen, "dead" space 11 of tile 24 in column (a) corresponds to an imaging surface of a tile 24 in column (b). During an imaging operation, the arrangement in Figure 3 is stepped
5 relative to the object to be imaged in a direction transverse, preferably substantially orthogonal, to the columnar direction of the tile array. By stepping the arrangement of Figure 3 in a transverse direction, during an image exposure, "dead" spaces 11 may be compensated for and substantially eliminated. However, such an arrangement requires a stepper mechanism for relative movement and image processing circuitry and
10 appropriate software for processing the resultant multi exposure image. Such imaging device tile systems are complex and run the risk of mechanical failure.

A further drawback of known configurations for imaging device tiles 24 is that the detector layer 1 is mechanically and electrically coupled to the circuit layer 3 by
15 low-temperature bump bonds. Bump bonds couple each detector cell to a corresponding detector circuit cell and consequently there is a high density array of bump bonds. For example, in this technology the order of bump bonds per square mm is generally in the range 4 to 40K bump bonds per square mm. Examples of the Applicant's devices have of the order 900 bump bonds per square mm. The following
20 table shows a spread of bump bond density for various devices.

Pixel Size – side dimensions of square in microns	Bump Bond Density in bumps per square mm.
500 – Gamma Camera	4
100 – Panoramic & Real-time Cassette	100
35 – High Resolution Silicon Sensor	900
10 – tested in laboratory	10,000
5 – technology road map	40,000

Table 1

It is extremely difficult to ensure and maintain consistent bump bond quality, particularly since the bump bonds cannot be inspected. These difficulties impact significantly on the quality and hence manufacturing yield of imaging devices and imaging device tiles.

5

The present invention is made with the foregoing considerations in mind.

In a first aspect of the invention there is provided a semiconductor circuit substrate, comprising active circuitry supported by said circuit substrate, and one or more conductive paths supported by said circuit substrate for supplying at least one of control, readout and power supply signals to and/or from said active circuitry, said one or more conductive paths extending from said active circuitry to an interface region of said circuit substrate. One or more signal pathways extend from said interface region through said circuit substrate to a surface of said substrate, said one or more signal pathways electrically coupled to said one or more conductive paths to provide an external signal interface for said active circuitry.

In a second aspect of the invention there is provided a method for fabricating a semiconductor circuit substrate, the method comprising the steps of:

(a) etching one or more signal pathways through a semiconductor circuit substrate from a surface thereof at a location corresponding to an interface region of said circuit substrate, said one or more signal pathways corresponding to at least one of control signal, readout and power supply lines for supplying at least one of control signal, readout and power to an active circuit supported by said circuit substrate; and

(b) depositing low impedance conductive material in said one or more signal pathways to provide one or more low impedance conductive signal pathways between said at least one of control signal, readout and power supply lines and a surface of said circuit substrate.

Suitable etch techniques are well known to the skilled person and include chemical etching, and plasma etching.

Embodiments in accordance with the present invention obviate the need to couple control, readout and power supply signals from the circuit substrate to a mount, such as a printed circuit board, with bond wires, since the signal pathways route the signals through the circuit substrate to a contact on a surface of the substrate. The contact on the surface of the circuit substrate may then be directly coupled to a corresponding contact on the mount. This is more reliable and robust than wire bonding the circuit substrate to the mount, removes a cause of the "dead space" which arises between known imaging device tiles if tiled together to provide a flat large area image surface. Thus for example, large numbers of imaging device tiles having a circuit substrate in accordance with the invention may be "butted up" against each other to provide a substantially continuous, yet flat, large area image surface. Furthermore, the method for fabricating circuit substrates in accordance with embodiments of the invention involves a "wafer level" process, which can be carried out during or after manufacture of the circuit substrate, and using a similar process to that used in manufacturing the circuit substrate.

Preferably, in the above method step (a) further comprises the steps of:

- (a)(i) depositing photo-resistive material over said circuit substrate;
- (a)(ii) applying a photo-lithographic mask having one or more openings corresponding in said interface region;
- (a)(iii) exposing said photo-resistive material through said openings in said mask;
- (a)(iv) removing said exposed photo-resistive material to expose said circuit substrate; and
- (a)(v) etching said exposed circuit substrate to etch said one or more signal pathways through said substrate.

The one or more signal pathways may be formed of a low impedance conductive material, which provides a relatively low loss and low noise transmission medium for the control, readout and power supply signals. A low impedance conductive material is particularly suitable for transmitting signals over relatively long distances, compared with typical interconnect distances in a semiconductor circuit substrate, such as is the case for external interface signal paths.

Typically, the signal pathways comprise a via hole which may be filled with the conductive material, or optionally the via hole internal walls are coated with the conductive material. Suitably the conductive material is a metallic material, in particular a metal or comprising a metal. The conductive material may also be made of layers of metals and/or metal alloys.

By reducing the depth of the circuit substrate in the interface region relative to the rest of the substrate the step (aspect) ratio of the via hole may be controlled. Typically a step ratio of 5:1 is desired. If a substrate is too thick to etch with such a step ratio, then it can be thinned. This avoids making circuit substrates which have very wide via holes at one end which would result in reduced useful circuit area. Preferably, the step of reducing the thickness of said circuit substrate in said interface region relative to the rest of the substrate is carried out prior to step (a) of the above described method.

Forming the interface region near to or including an edge of the substrate is a convenient location, since conventionally interfaces are disposed at one end of a substrate.

Conductive shielding, coupled to a reference potential such as ground for example, may be formed around a substantial part of said one or more signal pathways in order to shield the signal pathways from noise, such as "shot noise" from incident radiation, and cross-talk between adjacent signal pathways.

Preferably, forming the shielding comprises, prior to step (b), the steps of:

(b)(i) depositing a conductive shielding over internal walls of said one or more via holes; and

(b)(ii) depositing an insulating layer over said conductive shielding.

Conveniently, the circuitry is formed in a surface region of the circuit substrate opposing said circuit substrate region to which said one or more signal pathways extend. Forming the circuitry in a surface region makes it relatively straightforward to

couple another substrate, such as a detector substrate, to the circuitry. By having the surface in which the circuitry is formed opposing the surface to which the signal pathways extend results in the signal pathways having a substantially straight path making their manufacture relatively straightforward.

5

In one embodiment the circuitry comprises radiation detection circuitry which may detect radiation itself, or be configured to receive charge from a radiation detector cell which itself is responsive to incident radiation to generate charge. Such a detector cell may be disposed on a detector substrate separate from said circuit substrate, which
10 provides for the use of a detector substrate material optimised for a particular type of radiation.

In another aspect of the invention a radiation detection device is provided which includes a semiconductor circuit substrate as described above, and a detector substrate
15 including a detector cell responsive to incident radiation to generate charge, the detector cell including at least one detector cell contact for coupling charge from the detector cell to the detector cell circuit. This detection device may be used as a simple radiation detector, or as the radiation detection element in a "Geiger counter".

In another aspect the circuitry comprises an array of detector cell circuits associated with a corresponding array of detector cells, each detector cell responsive to radiation incident thereon to generate charge, and wherein respective detector cell
20 circuits of the array of detector cell circuits are configured to receive charge from associated detector cells of the array of detector cells. Such an arrangement may be used to make an imaging device for imaging radiation, comprising a detector substrate including an array of detector cells each including a detector cell contact for coupling
25 charge from the detector cell, and wherein respective detector cell circuits of the array of detector cell circuits are configured to receive charge from the detector cell contacts of associated detector cells of the array of detector cells.

30

These devices may have a separate detector substrate optimised for the type of radiation for which they are to be used.

The circuitry may be of any suitable type for implementing different radiation detection or imaging device applications. For example the circuitry may include one or more of the following: charge accumulation circuitry; counter circuitry; read out
5 circuitry; energy discriminator circuitry; pulse shaping circuitry; pulse amplifying circuitry; analogue to digital converter circuitry; and rate divider circuitry.

The detector substrate suitably comprises a bias contact on a surface thereof opposing the detector cell contact, the bias contact defining the detector cell in co-
10 operation with said detector cell contact, and for an imaging device the detector substrate a plurality of detector cell contacts defining an array of detector cells in co-operation with the bias contact.

Particular embodiments include a radiation detection device tile, comprising:
15 a radiation detection device such as described above; and
a mount for mounting the detection device;
the mount including contacts for conductively coupling the conductive signal pathways to corresponding external signal lines disposed on the mount.

20 Another embodiment includes a radiation imaging device tile, comprising:
a radiation imaging device as described above; and
a mount for mounting said detection device;
the mount including contacts for conductively coupling the conductive signal pathways to corresponding external signal lines disposed on the mount.

25 Utilising various embodiments in accordance with the invention a radiation imaging cassette may be formed, comprising a housing, and a plurality of radiation imaging device tiles as described above. The radiation imaging device tiles may be mounted and arranged to form a large area imaging tiled array. A radiation cassette as
30 just described is a suitable plug-in replacement for a conventional film cassette. Thus, solid state digital imaging may be provided for legacy imaging systems, hitherto operable for just film. This removes the need for re-engineering of existing systems to

fit semiconductor based digital imaging systems, and also reduces the need to replace such systems due to obsolescence as they can be relatively easily updated for digital imaging by using a radiation imaging cassette in accordance with the invention, and connecting it to a suitable image processing apparatus such as a computer.

5

Illustrative embodiments of the present invention will now be described, hereinafter by way of example only, with reference to the accompanying drawings in which like numerals refer to like elements, and in which:

10 Figure 1 is a schematic illustration of known imaging device tiles;

Figure 2 is a schematic illustration of known imaging device tiles tilted to provide a substantially continuous imaging surface;

Figure 3 schematically illustrates a known configuration of an array of imaging device tiles having columns offset in a columnar direction;

15 Figure 4 schematically illustrates an imaging system using an imaging device in accordance with an embodiment of the present invention;

Figure 5 is a cross section of one example of an imaging device;

Figure 6 is a schematic circuit diagram of an example of a detector cell circuit;

20 Figure 7 is a schematic circuit diagram of a further example of a detector cell circuit;

Figure 8 is a schematic block diagram of a yet further detector cell circuit;

Figure 9 is a schematic illustration of the bump-bond connections for a known imaging device mounted to an imaging support;

25 Figure 10 is a schematic illustration of one embodiment of the invention using conductive via holes;

Figure 11 is a schematic illustration of another embodiment of the invention using conductive via holes;

Figure 12 schematically illustrates an arrangement for "thinning" a CMOS circuit substrate;

30 Figure 13 provides a series of drawings illustrating the steps for forming a circuit substrate in accordance with an embodiment of the invention;

Figure 14 is a schematic illustration of an imaging device using conductive via holes to couple a detector substrate to a circuit substrate;

Figure 15 is a detailed schematic illustration of the arrangement illustrated in Figure 14.

5 Figure 16 provides a series of drawings illustrating the steps for forming an imaging device substantially as illustrated in Figures 14 and 15 ;

Figure 17 schematically illustrates plural imaging devices in accordance with an embodiment of the invention placed "end-to-end" in a tiled arrangement;

10 Figure 18 schematically illustrates plural imaging devices substantially as illustrated in Figures 14 and 15 placed "end-to-end" in a tiled arrangement;

Figure 19 schematically illustrates a radiation imaging cassette utilising a 3×3 array of imaging devices in accordance with an embodiment of the present invention; and

15 Figure 20 schematically illustrates an imaging system utilising a radiation imaging cassette as illustrated in Figure 19.

Figure 4 is a schematic block diagram of one example of an imaging system using an imaging device in accordance with the present invention. This particular embodiment is directed to the imaging of high energy radiation, for example X-ray radiation. By high energy radiation is meant radiation having an energy in excess of approximately 1 KeV. However, the invention is by no means limited to high energy radiation such as X-rays but could be applied to the detection of any particular radiation, for example γ -ray, β -ray, α -ray, infra-red or optical radiation, subject to an appropriate choice of semiconductor detector substrate.

25

The imaging system 30 of Figure 4 is shown to provide imaging of an object 32 subject to radiation 34. In this example the radiation may, for example, be X-ray radiation as mentioned above, but could optionally be γ -ray, β -ray, or α -ray radiation for example. The object 32 may, for example, be part of a human body. The imaging device 36 comprises plurality of image cells (here image cells 38 of a two dimensional image cell array). In the following, reference will be made to image cells in a two dimensional array although it will be appreciated that in other embodiments the

30

individual image cells may have a configuration other than within a two dimensional array (e.g. a strip arrangement).

5 The imaging device detects directly high energy incident radiation and accumulates at each image cell, a charge corresponding to, or count of, the incident radiation hits at that image cell. The imaging device 36 is configured on two substrates, one with an array of detector cells 39 and one with an array of corresponding detector cell circuits 40, the substrates being mechanically connected to each in accordance with an embodiment of the invention.

10

Control electronics 42 provides control signals to, and readouts image signals from, the imaging device 36 over bus 48, and outputs an image over bus 50 to a display device such as a cathode ray tube or LCD display 52. Image processor 46 and display device 52 are controlled by input devices 54 such as a keyboard or pointing device (mouse) by way of control signals over buses 56 and 58 respectively.

15

The imaging system 30 may have many applications, including but not limited to the following examples:

20 X-ray mammography; intra-oral X-ray imaging; panoramic oral X-ray imaging; computerised axial tomography (CAT); PET scanning; autoradiography; high speed real-time fluoroscopy; Gamma camera imaging; security baggage screening; spectroscopic imaging; X-ray diffraction crystallography; and non-destructive inspection.

25

Although only one imaging device 36 is shown, it will be appreciated that more than one imaging device may be utilised for example configured as an array of imaging device tiles.

30

Figure 5 is a schematic cross-section of part of a known imaging device 36. In this example, the imaging device 36 comprises a detector substrate 60 connected to a detector cell circuit substrate 62 by means of bump-bonds 64. A detector cell 39 of each image cell 38 is defined on the detector substrate 60 by a continuous electrode 66

which applies a biasing voltage and image cell location electrodes 68 to define a detection zone for the image cell 38. Corresponding active detector cell circuits 70 on the detector cell circuit substrate 62 are defined at locations corresponding to the electrodes 68 (i.e. the detector cells 39). The detector cell circuits 70 are electrically
5 connected to the corresponding electrodes 68 by bump-bonds 64 which form a conductive pathway. In this manner, when charge is generated in a detector cell 39 in response to incident radiation, this charge is passed via the bump bond 64 to the corresponding detector cell circuit 70.

10 The actual size of the detector cell circuit and the detector cell will depend on the application for which the imaging device is intended, and will also depend on the integrated circuit technology available for constructing the detector cell circuit 70. With current circuit technology, it is not possible to obtain the smallest possible image
15 detectors which would be required in some applications. Typically, the minimum image cell size is of the order of 200 square micrometres using current technology. However, with advances expected in circuit manufacturing technology, it is expected that this minimum size can be significantly reduced using the teaching of the present application and improved circuit fabrication techniques. Accordingly, the present invention is not limited to any particular image cell size.

20

Any appropriate semiconductor materials can be used for the substrates. For example, silicon may be used for the detector substrate and for the circuit substrate. Other semiconductor materials could be used. For example, for the detector substrate, the material could be selected from: CdZnTe, CdTe, HgI₂, InSb, GaAs, Ge, TiBr, Si
25 and PbI.

Figure 6 illustrates one example of a detector cell circuit 70 for an image cell in an example of an imaging device suitable for use in an embodiment of the invention. This example of a detector cell circuit uses field effect transistors (FETs) arranged as a
30 cascode connected amplifier. VBIAS 80 is a bias voltage input across the depletion zone forming the detector cell 39 of the image cell. The detector cell 39 is represented by the diode symbol D11. In the detector cell circuit itself, SIGOUT 82 is an analogue

signal output and VANA 84 an analogue power supply input. RES-R-1 86 is a reset input and ENA-R-1 88 is an enable input for the detector cell circuit. Charge is accumulated in the gate of a transistor M11A 90 when both the RES-R-1 86 and ENA-R-1 88 inputs are low.

5

The gate capacitance substantially forms the input node capacitance (total capacitance) thus maximising charge storage ability. In this example it is an aim of the detector cell circuit configuration to provide maximum charge accumulation ability by minimising the parasitic or unwanted capacitance of all other circuit (and detector) components and forming substantially all input node capacitance from the charge accumulation transistor M11A 90. Other detector cell circuits configurations may be optimised for fast read, and seek to reduce or optimise capacitance throughout the cell circuit to provide for such fast read out. For a 35 μm by 35 μm detector cell circuit the M11A 90 capacitance can be 2pF and the FET gate voltage dynamic range can be at least 2 Volts. This corresponds to about 25,000,000 electrons in storage capacity which is more than 100 times the capacity of a CCD of the same image cell size. It should be noted that the 2pF of the FET capacitance in the above example substantially forms all of the input mode capacitance of the image cell. In the above example of 35 by 35 μm pixels the total parasitic capacitance of the detector and the other elements in each detector cell circuit and corresponding detector cell is in the range of a few fF or tens of fF. For a charge accumulation circuit the capacitance of the charge storage device should be maximised and in any case be substantially bigger than the parasitic capacitance in each image cell. In the example above the capacitance of the FET acting as charge accumulating device in the detector cell circuit is more than 90% of the total capacitance of the image cell comprising a detector cell and the corresponding detector cell circuit. As a result of this, substantially all collected charge will be accumulated in the charge accumulating FET rather than being shared among the rest of the detector cell circuit elements. Optionally, the capacitance may be more evenly distributed throughout the detector cell circuit, and for fast read out applications the capacitance of the detector cell circuit may be significantly lower than that of circuitry optimised for charge accumulation. It will be appreciated that the use of a FET provides one example only, of a detector cell circuit

in which example charge accumulating capacitance is maximised using a charge storage device (such as a FET gate of a capacitor) that accounts for most of the input node capacitance for each image cell.

5 To read the image cell, ENA-R-1 is taken to a high state, which allows current to flow from the transistor M11A 90 through the transistor M11B 92 to SIGOUT 82. The detector cell circuit is reset by taking RES-R-1 86 to high, whereupon after RES-R-1 has been at high for merely a few microseconds, any accumulated charge will have been removed from the gate of the transistor M11A 90. Immediately after RES-
10 R-1 goes to a low level, charge can begin to accumulate at the gate of the transistor M11A 90. If no reset pulse is supplied to the reset input RES-R-1 86, then it is to be noted that a reading operation when the enable input ENA-R-1 goes high does not destroy the charge but instead merely causes a current flow directly proportional to the accumulated charge. This allows multiple readings without resetting.

15

Figure 7 illustrates a further example of detector cell circuit 120 for an image cell. This example is similar to the example of Figure 6. The detector cell is represented at PD 119 of the image cell. In the detector cell circuit itself, VBIAS 122 is a voltage bias, OUT 182 is an analogue signal output, RESET 186 is a reset input
20 connected to a reset FET 147 and ENABLE 188 is an enable input connected to an enable FET 192 for the detector cell circuit. Charge (electrons) is (are) accumulated in the gate of a charge storage FET 190 when the ENABLE 188 input is low and the RESET 186 input is high. To read the detector cell circuit ENABLE 188 is taken to a high state, which allows current to flow from the FET 190 through the FET 192 to
25 OUT 192. The detector cell circuit is reset by taking RESET to low, whereupon after RESET 186 has been at low for merely a few microseconds, any accumulated charge will have been removed from the gate of the FET 190. Immediately after RESET 186 goes to a high level, charge can begin to accumulate at the gate of the FET 190. If no reset pulse is supplied to the rest input RESET 186, then it is to be noted that a reading
30 operation when the enable input ENABLE goes high does not destroy the charge but instead merely causes a current flow directly proportional to the accumulated charge. It will therefore be seen that the operation of the circuit of Figure 7 is similar to that of

Figure 6. In addition, the circuit of Figure 7 includes diodes 154 and 156 which act as overload protection circuitry for the detector cell circuit. The diodes provide protection both against static electricity which might damage the FETs and against FET overload. The FET gate 190 accumulates more than a predetermined charge threshold (e.g. corresponding to 5 volts, which is the voltage bias) then current will start to flow through the diode 156 towards the ground thus protecting the FET 190. This will protect detector circuit cells which, for example, receive a full radiation dose outside the perimeter of an object to be imaged. Preferably the two FETs 190 and 192 are implemented as a cascode amplifier stage. In this configuration the two FETs 190 and 192 provide impedance-up conversion without increasing the noise accordingly. Consequently, the noise level from each detector cell circuit described in the current embodiment is only about 500 e while the detector cell circuit retains very small size (as small as 10-20 μm image cell size), very large dynamic range of 50,000,000 e and individual addressability.

Figure 7 also illustrates an optional bipolar transistor 160, which may be omitted. The purpose of the bipolar transistor, with its connection to a voltage source VBASE, will be described later.

In addition to the features already described above, optional features may be included in the image cells and/or devices which can be used for isolating individual detector circuits in a manner to be described below.

For different detector cells the corresponding charge storing FETS 190 may accumulate different amounts of charge as a result of the different radiation or light intensities incident upon the detector cells. Consequently, a potential difference is created between adjacent image cells. If the image cells are not electrically separated this potential drop may cause signal charge to leak from one detector cell circuit through the detector and into the neighbouring detector cell circuit. The longer the accumulation time, the more severe the problem could be. In accordance with one embodiment of the invention, this effect is diminished or eliminated by providing means for electrically separating, or equivalently maximising the resistance of adjacent

image cells. Accordingly, a passivation layer, for example of polyamide or of aluminium nitride, is applied between detector cells (i.e. between the electrodes 68 that define the detector cell). This electrically separates adjacent detector cells since such a passivation is non-conductive. Additionally, electrodes may be applied on the
5 passivation layer and an applied voltage V will create a barrier potential penetrating several micrometers inside the detector cell volume 39. Thus charge attempting to escape from the charge accumulating FET in a detector cell circuit 38 will encounter the barrier potential and will not be dissipated into the adjacent detector cell circuit FET.

10

Furthermore, a third option is to provide an npn transistor (bipolar transistor 160) at the entrance of each detector cell circuit. This is shown in Figure 7. When the base of the bipolar transistor is set at an appropriate voltage common to all bipolar transistors of the detector cell circuits (about 1V) the bipolar transistor will act as a
15 diode allowing charge to flow into the gate of the FET 190 but at the same time prohibiting any escape along the reverse path. In this way, while maintaining different potential drops at the gates of the charge accumulating FETs 190 (proportional to the different signal charges that have been accumulated), the potential at the entry of the detector cell circuits is common to all detector cell circuits. Thus, means are provided
20 to electrically separate image cells in the imaging device so as to retain all or substantially all charge accumulated on each detector cell circuit. This is particularly useful when accumulation times are rather long, for example in the range of tens or hundreds of microseconds and even more useful when accumulation times are in the range of msec or tens or hundreds of msec.

25

Figure 8 is a schematic diagram of another example of an individual detector cell circuit 220 as disclosed in International Patent Application Publication No. W098/16853, corresponding to US Patent No. 6,248,990 incorporated herein by reference. The detector cell 39 is represented by the diode in Figure 8. The input
30 to the detector cell circuit 220 corresponds to the conductive path connection 64 between the detector cell 39 and the detector cell circuit 70 illustrated in Figure 5.

When a photon is photo-absorbed in a detection zone of the detector cell 39 creating an electric charge, or when a charge radiation ionises a detection zone of the detector cell 39, an electric pulse flows from the detector cell 39 via the bump-bond 64 to threshold circuitry 242 of the pixel circuit 220. The threshold circuitry 242 effectively filters the input radiation intensity by comparing the input pulse peak to one or more threshold values. The output of the threshold circuitry 242 is connected to counter circuitry 244 for counting pulses (radiation hits) within one or more predetermined ranges as defined by the threshold circuitry, thereby implementing incident photon energy discrimination. The counter circuitry is connected to counter circuitry of other (typically adjacent) detector cell circuits for readout purposes via connections 232 and 234. Various inputs to the detector cell circuits 220 include hold 252, load 254, enable 256, reset 258 and clock 292 signal lines and voltage supply lines Vdd and Vss (not shown).

One or more imaging device tiles 24 may be mounted on an imaging support 8 as illustrated in Figure 9. The imaging support 8 not only provides a mechanical support for imaging device tiles, but also circuitry and signals lines for imaging devices as will now be described.

Each imaging device 20 has tens of thousands of pixels but only needs around 5-15 external lines to provide control signals, supply voltage and readout the signals. These lines are provided on the PCB 4 and also, for example, on a circuit board 8 on which the imaging device tile 24 may be mounted. The imaging device 24 itself carries a number of contacts 6 in the form of, for example, small metal spheres or bumps. The number of contacts typically corresponds to the number of external lines. The metal bumps 6 match an equal number of small appropriately sized contacts 7 on the circuit board 8 of the imaging support. The contacts on the circuit board 8 of the imaging support are connected to the aforementioned control, supply and signal lines (not shown). It will be noted in Figure 9, that there are two steps at the left hand end of the imaging device. The first step 12 is between the detector 1 and the readout chip 3, and the second step 14 is between the readout chip 3 and the mount 4. The purpose of these steps is to enable the connection of bond wires 10 between contact pads on the

readout chip 3 and respective contact pads on the mount 4. This provides for the external electrical interface of the readout chip 3 to the metal bumps 6 mentioned previously. In the readout chip 3, all internal electrical connections are brought to a single end of the chip to facilitate this connection and also to reduce the amount of dead imaging area for a mosaic of imaging device tiles. It will be appreciated that when the imaging devices tiles are arranged side-by-side and end-to-end, dead spaces (i.e. areas over which the detector does not extend) occur at the stepped region described above. Also, in conventional tiled arrays, spaces between adjacent imaging devices arranged side-by-side occur as the supports are wider than the detector surfaces.

As described hereinbefore approaches to dealing with this problem have been proposed which involve staggering adjacent rows of imaging devices on an imaging array and then providing for relative movement between an object to be imaged and the imaging array. This means that the effect of the dead spaces can be at least substantially eliminated, but this does require the provision of the mechanism for the relative movement and appropriate software for processing the resultant multi-exposure image. Another approach to dealing with this problem is to modify the structure of the individual tiles to enable adjacent tiles to be mounted very close to or even touching each other. The tile structure is arranged such that the imaging device is tilted with respect to the mount 4 and/or the support plane 8. A portion of the imaging device 20 may therefore be arranged to overlap the dead space of an adjacent imaging device tile in order to provide a substantially continuous imaging surface, such as illustrated in Figure 2. The tiles can be connected both electrically and mechanically to the support plane in, for example, one of the ways described above, although other suitable mounting techniques could be employed.

As will be appreciated from a reading of the foregoing description, various configurations of arrays of imaging device tiles may be formed to provide a large area imaging surface, and overcome the common problem of "dead" space at one end of an imaging device tile caused by the bond wires 10 between the circuit substrate 3 and printed circuit board 4. However, these arrangements are mechanically complex, and

/or require significant signal processing, and/or provide sub-optimal imaging, e.g. optical characteristics.

5 Generally speaking, embodiments of the present invention utilise an electrically conductive signal pathway between major surfaces of the circuit substrate, to make electrical connections between the circuit substrate and mount 4 without bond wires, thereby avoiding "dead" imaging space of the ends of an imaging device. The conductive signal pathway is made by etching a hole (via hole) through the circuit substrate between the surfaces of the substrate, and either coating the surface of the
10 hole with electrically conductive material, or providing an electrically conductive in-fill for the holes.

Embodiments of imaging devices in accordance with aspects of the present invention by way of non-limiting examples will now be described.

15

Figure 10 illustrates a first embodiment in accordance with one aspect of the invention, comprising an imaging device 320 formed of a detector substrate 60 having a detector cell contact 68 flip chip bonded to a detector cell circuit substrate 362, (the flip chip bond is shown in exploded form for clarity). The detector substrate 60 is flip
20 chip-bonded to the circuit substrate 362 via bump bonds 64 which are built on circuit contacts of detector cell circuits 70. The control signal, readout signal and supply voltage lines 361 for the circuit substrate 362 are arranged so that they terminate in an interface region at one end, 326, of the circuit substrate 362. However, circuit substrates in accordance with embodiments of the present invention need not have
25 their control signal lines brought to one end or side of the circuit substrate, but may have them at any region within the circuit substrate.

In circuit substrate 362 interface region 326 a series of via holes 321 forming signal pathways are etched through the circuit substrate 362 to provide a conduit
30 between the detector cell circuit layer and the bottom layer, typically between respective major surfaces of substrate 362. Contact pads 322a and 322b may be formed on respective surfaces of the circuit substrate 362 and coupled together via a

conductive infill 322 such as gold, thereby providing a low impedance conductive pathway between respective major surfaces of substrate 362. Other suitable conductive materials may be used such as silver, copper, aluminium, tungsten and TiN. Typically, the contact pads 322a and 322b will be formed at the same time as
5 conductive infill 322, and by way of the same process step. Contact pad 322a is connected to a control, signal and/or supply voltage line for the detector cell circuit 70. Contact pad 322b is formed to provide a suitable contact point to electrically couple to contact 328 of mount 4.

10 Optionally, the walls of the via hole may be coated with a conductive material to provide the conductive signal pathway.

As is clearly illustrated in Figure 10, the use of conductive through via holes in circuit substrate 362 removes the need for bond wires between the circuit substrate 362
15 and mount 4. Thus, the ends of the detector substrate 60, circuit substrate 362 and mount 4 may lie along the same line. A device tile 324 comprising such a detector substrate 60, circuit substrate 362 and mount 4 may be placed and butted directly against an adjacent similar imaging device tile. Thus, a substantially continuous imaging surface may be achieved, which is flat, and does not require elements for
20 tilting imaging device tiles.

The step ratio of via holes etched through circuit substrates such as silicon (Si), or Gallium Arsenide (GaAs), Sapphire, and other III-V class substrates are such that for a circuit substrate thickness of 50 to 300 microns the diameter of the via hole at one
25 surface will be of the order 30 microns for a diameter of 20 microns at the opposite surface. In general a width to depth (aspect) ratio of about 5:1 is used. The width to depth ratio is an important parameter for the via holes since it determines the ease with which the via holes may be through plated or filled with conductive material. Additionally, the step ratio determines the diameter of the via hole at one of the
30 surfaces which if too large would take up too much of the surface area of the corresponding circuit substrate 362 or mount 4 to be useful. The limit on how thin a circuit substrate may be is determined by the depth to which circuits extend into the

substrate. With current technologies the maximum depth is about 50 microns, but the invention is not limited to such technologies. Typically, the substrate thickness is of the order 100 microns.

5 Figure 11 illustrates a second embodiment of the present invention which seeks to ameliorate the problems associated with a step ratio that is too great for efficient utilisation of the mount 4 or circuit substrate surfaces. A circuit substrate 363 is "thinned" in the interface region 326 to which the control, signal and supply voltage lines for circuits 70 are terminated on the surface of circuit substrate 364. Mount 4
10 requires an upstanding mount contact 328 in order to compensate for the thinned region of circuit substrate 364. Optionally, of course, mount 4 may be profiled in order that contact 322b of circuit substrate 364 may electrically couple to a flat profiled mount contact 328.

15 Optionally, the whole of circuit substrate 362 may be thinned in order to achieve an effective step ratio for the through via holes 322. A circuit substrate 362 thinned across its whole surface would look substantially the same as circuit substrate illustrated in Figure 10, but thinner.

20 Thinning the whole surface of circuit substrate 362 is a more simple process than seeking to thin just the edge region 326. For an automated process which is reliable and repeatable, thinning the whole of substrate 362 is preferable to thinning just a small region.

25 In a preferred embodiment of the invention, circuit substrate 362, 364 is thinned prior to having the via holes etched through it in order to provide an appropriate step ratio of about 5:1. Suitably, detector cell circuits 70 are fabricated on circuit substrate 362, 364 after via hole etching, or thinning and via hole etching. Optionally, the detector cell circuits 70 may be formed on the circuit substrate 362,
30 364 prior to the etching of the through via holes, or thinning and via hole etching of the circuit substrate. Generally, the circuit substrate is thinned prior to etching, although thinning may take place after etching. When thinning is performed after

etching it is not necessary for the etch to go through the whole of the substrate, since the thinning process can take off any unetched layer thereby exposing the via hole.

5 An example of a method of fabricating an imaging device in accordance with an embodiment of the present invention will now be described.

Figure 12 illustrates an arrangement for "thinning" a silicon wafer 420 prior to etching. The wafer 420 is mechanically lapped to a thickness of approximately 100 to 150 microns. Typically, this lapping is done by standard backgrind or Chemical
10 Mechanical Polishing (CMP) process, both of which involve a rotating platen having suitable abrasiveness to provide a polishing pad 422. The polishing particle size is of the order 35 of microns. The wafer 420 is held in a rotating chuck assembly 424 comprising a retaining ring 426 for fixing the wafer in the chuck assembly 424, and a carrier member 428 for supporting the retaining ring 426. The carrier member 428
15 attached to a spindle 430 via which a rotating motion may be applied to the chuck assembly 424. Additionally, the rotating chuck assembly 424 may be moved back and forth across the polishing pad 422. An abrasive slurry may be introduced between the polishing pad 422 and wafer 420 for assisting in and lubricating the mechanical grinding process. A down force is applied via spindle 430 to hold the wafer 420
20 against polishing pad 422.

Although optimum grinding and polishing may be achieved by rotating both the wafer and the polishing pad, a suitable and grinding polishing arrangement may comprise only one or other of the wafer or polishing pad being rotated whilst the other
25 part remains stationary, or may moved back and forth relative to the polishing pad.

Wafer 420 may be a substantially unprocessed "raw" wafer typically 6 inches diameter having a number of detector circuit substrate "chips" fabricated on it. Optionally, individual detector circuit substrate chips previously cut from a "raw"
30 wafer may be individually polished and ground.

A process for fabricating an imaging device having conductive via holes for providing an external interface to a circuit substrate will now be described with reference to Figure 13 of the drawings. Although only one conductive via hole and signal line is illustrated, it will be evident to the person of ordinary skill in the art that the process may be applied for a plurality of conductive via holes and signal lines.

Figure 13A illustrates a part of a "thinned CMOS" circuit substrate 362 including a control signal, readout signal or voltage supply line 361. As shown in Figure 13B, photo-resist 602 is deposited over the CMOS circuit substrate, including the supply line 361. The photo-resist 602 is then exposed through a suitable photolithographic mask to leave an area of the supply line 361 uncovered as illustrated in Figure 13C. Typically, the photo-resist 602 is exposed to leave 30-micron holes through the supply line 361. A 30-micron hole would give a 5:1 aspect ratio for a through via hole in a 150-micron thick circuit substrate. This should yield through holes having substantially clear, straight sidewalls. Evidently, other suitable dimensions for the hole diameter and substrate (wafer) thickness may be used. Additionally, the holes need not be circular, but may be oval, or have straight sides or be in the form of a square or rectangle for example.

The circuit substrate 362 is then etched through the exposed regions of the photo-resist 602, for example using a typical industry standard process such as a $\text{SF}_6/\text{O}_2/\text{HBr}$ type process, to produce through via hole 321 in the circuit substrate 362, as illustrated in Figure 13D. The photo resist will then be removed from the detector circuit substrate.

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A photo resist layer 604 is deposited over the circuit substrate, including the side walls of the via hole 321. Subsequently, a mask is placed over photo resist 604, and the photo resist exposed to leave uncovered the region corresponding to the via hole 321, including the side walls, as illustrated in Figure 13E. In the next step, gold 606 is deposited over the circuit substrate as illustrated in Figure 13F. As can be seen in Figure 13F, gold is deposited on the remainder of the supply line 361 and along the side walls of the via hole 321 to the lower surface 608 of the circuit substrate, thereby

providing electrical coupling between the supply line 361 and the lower surface of the circuit substrate. Gold 606 may be deposited via any suitable means. For example sputtering, electrical chemical deposition, E-Less, or Electro-Less or Electric-less chemical deposition.

5

Photo-resist 604 is subsequently removed, thereby removing the excess gold, as illustrated in Figure 13G. In the particular arrangement illustrated in Figure 13G the side walls of the through via hole 321 are coated with conductive material. Evidently, more gold could be deposited in the step illustrated in Figure 13F to create a more solid in-fill of through via hole 321. However, such extra in-fill is not necessary and would lead to unnecessary expense.

10

The applicant has discovered a drawback with using thinned circuit substrates to manufacture imaging devices. A thinned substrate is considerably weaker than a substrate as usually provided, and is prone to cracking or even breaking during the bump bonding of a detector substrate 60 to it. Bump bonding of thinned circuit substrates results in a high level of damaged substrates and consequently an unacceptably low yield during the manufacture of imaging devices 320.

15

The problem with bump-bonding to thinned circuit substrates has been addressed by the applicant by way of the synergistic application of the foregoing described technique to provide a means of electrically, and optionally mechanically, coupling a detector substrate to a circuit substrate.

20

By way of a general teaching, the approach is to have a readout circuit substrate (IC circuit) which is thinned and has via holes. The through via holes are disposed near the contact areas of the readout circuit (wafer). Via holes are based on the well-known etching behaviour of circuit substrates e.g. silicon. The general idea is to stack the IC circuit on top of the detector and fill the via holes with metal. The filled via hole works as a connection between the IC and detector substrate. The filling of the holes can be done with sputtering, chemical or electro-chemical coating. Such a method does not require expensive flip chip or wire bonding, or suffer from the

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“dead” spaces resulting from wire bonding. Furthermore, it is a wafer level process. This results in the new possibility of tiling devices closely together.

5 The basic arrangement of an imaging device and imaging device tile configured in accordance with this further aspect is illustrated in Figure 14. The arrangement illustrated in Figure 14 includes a detector substrate 60 having a continuous bias electrode 66 on one surface, and detector cell contacts 68 formed on another surface to define detector cells. The detector substrate 60 is mechanically coupled to the circuit substrate 380 by way of a suitable adhesive material 382. The
10 adhesive material 382 could be any suitable material for mechanically coupling detector substrate 60 to the circuit substrate 380. For example, photo-resist, adhesive or epoxy, suitably patterned to leave the regions corresponding to detector cell contact 68 exposed. Circuit substrate 380 has via holes 384 etched through it and corresponding to detector cell contact 68 locations. Detector cell circuits 70 are
15 located adjacent each via hole 384 on the opposite surface of the circuit substrate to the adhesive material 382. Preferably, circuit substrate 380 has been thinned so that the via hole step ratio is not too large.

A conductive material is deposited onto detector contact 68 through via holes
20 384 in order to fill the via hole with the conductive material. Optionally, just the surface of the via hole is coated with conductive material 386. The conductive material may comprise gold, silver, copper, or other suitable conductive material such as Aluminium, Tungsten and TiN. Preferably, the circuit substrate 380 is thinned prior to having the via holes etched through it in order to provide an appropriate step ratio of
25 about 5:1. Suitably, detector cell circuits 70 are fabricated on circuit substrate 380 after via hole etching, or thinning and via hole etching. Optionally, the detector cell circuits 70 may be formed on the circuit substrate 380 prior to the etching of the through via holes, or thinning and via hole etching of the circuit substrate 380. Generally, the circuit substrate is thinned prior to etching, although thinning may take place after
30 etching. When thinning is performed after etching it is not necessary for the etch to go through the whole of the substrate, since the thinning process can take off any unetched layer thereby exposing the via hole.

The conductive material 386, either completely filling the via hole 384 or just coating its surface, is coupled to associated detector cell circuit 70. In this way charge
5 collected at detector contact 68 can be coupled via the conductive material 386 to the detector circuit 70.

Control and readout signal lines, and supply voltage lines are coupled from the detector circuits 70 to a circuit substrate contact pad 390. The circuit substrate contact
10 pad 390 provides electrical coupling to a mount contact pad 328 on mount 4. An epitaxial layer 388 is deposited over the lower surface of the circuit substrate to protect the detector circuit 70 and conductive material 386, and to electrically insulate it. The imaging device 420, formed of detector substrate 60 and circuit substrate 380 is coupled to mount 4 by way of a suitable adhesive material 392 thereby forming an
15 imaging device tile 424.

Since the detector cell circuits 70 are formed on the lower surface of circuit substrate 380, the control and readout signal lines, and voltage supply lines can run along the lower surface and therefore the circuit substrate contact pad 390 can also be
20 on a lower surface. Thus, there is no need to run bond wires from the top surface, i.e. the surface closest to the detector substrate, of circuit substrate 380 to a contact pad on mount 4, which as disclosed in previous devices requires the mount 4, circuit substrate and detector substrate to be stepped resulting in "dead" spaces. No such "dead" spaces are created in the arrangement disclosed in Figure 14.

25

Furthermore, the detector circuits are disposed further away from incident radiation than in the prior art configurations for the embodiments of the present invention described above with reference to Figures 10 and 11. Any radiation has to pass through the bulk of the circuit substrate material. This results in improved
30 radiation hardness of the detector circuit 70 due to there being substrate material, for example 120 microns of silicon, before the circuits which absorbs at least some of the radiation, such as X-rays, before it reaches the circuits themselves.

Yet further, bonding of the detector substrate to the circuit substrate has been achieved without bump-bonding, thereby reducing the chances of a thinned circuit substrate cracking during fabrication of an imaging device.

5

Figure 15 schematically illustrates a cross section taken through conductive via holes of an imaging device according to the arrangement described with respect to Figure 14. A detector substrate 60 has a bias contact 66 disposed on an upper, or radiation facing, surface (second major surface) of the detector substrate 60. The lower surface (first major surface) of the detector substrate 60 comprises an array of detector contacts 68. The resistance between the bias contact 66 and detector contact 68 is of the order $330\text{ G}\Omega$, and the inter-detector cell contact resistance is of the order $10\text{ G}\Omega$. In the embodiment illustrated in Figure 15, detector substrate 60 is mechanically coupled to the circuit substrate 380 by an adhesive material 382, which may be photo-resist, an epoxy resin or an adhesive. Via holes 384, etched through the substrate material 380 correspond to detector cell contact regions 68, and are filled with conductive material 386.

The conductive material 386 is electrically coupled to a corresponding detector cell contact 68. Although the illustrated embodiment shows a conductive in-fill, it is not necessary to completely fill the via hole with conductive material, but provide a suitable conductive coating around the via hole, or part thereof, which extends to a respective detector contact 68. The conductive material 386 extends to a circuit contact 392, for electrically coupling detector contact 68 to a detector cell circuit 70. The detector cell 70 is formed in the circuit substrate 380, which is typically a CMOS circuit.

A conductive shielding 394, typically of aluminium but which may be of any suitable conductive material, is deposited over the surfaces of the circuit substrate 380, including the walls of the via holes 384. The lower surface (first major surface) of the detector circuit substrate 380 has suitable gaps in the conductive shielding 394 for the

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detector circuit cell circuits 70 and corresponding detector cell circuit contacts 392. The conductive shielding 394 is coupled to a reference potential, typically ground.

5 An insulating material, 396, such as silicon oxide is deposited over the conductive shielding. The silicon oxide insulating material is typically of the order of five microns thick. An epitaxial layer 388, for example SiO_2 , is deposited over the lower surface of the detector substrate 380 to protect the detector cell circuitry surface and connections. A passivation layer 389 is deposited between detector contacts 68 in order to increase intercontact resistivity. Preferably, the passivation layer is aluminium
10 nitride.

The arrangement illustrated in Figure 15 comprises parasitic capacitance 398 between detector cell contact 68 and corresponding shielding 394. A further parasitic capacitance 400 exists between shielding 396 and the bulk detector substrate material
15 in the CMOS detector cell circuit region. Although parasitic capacitances are generally considered undesirable since they tend to reduce detector charge collection efficiency, limit maximum operating speed, can introduce "cross-talk" between adjacent detector cell circuits, increase readout signal noise and interconnect signal path impedance, in the present embodiments such drawbacks are tolerated due to the
20 advantages provided by the arrangement of Figure 15. Furthermore, thinning a circuit substrate reduces the parasitic capacitance between the detector substrate and circuit substrate.

For an embodiment such as illustrated in Figure 15, the circuit substrate 380
25 has been "thinned" down from its usual thickness. Typically, circuit substrate material 380 is supplied as a wafer, or a die thereof, 600 microns thick. After thinning, the circuit substrate material 380 is of the order of 100 microns thick. The reduced thickness of the circuit substrate material results in a surprising yet beneficial reduction in electronic noise.

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Sources of noise in an imaging device such as illustrated in Figure 15, amongst other things, are electron-hole pairs created by high energy radiation passing through

detector substrate 60 and being incident on the circuit substrate material. Whilst the material for the detector substrate 60 is chosen for the high number of electron-hole pairs (of the order of 20,000 electron whole pairs) generated by incident high energy radiation, it is desirable that the circuit substrate material produce substantially fewer
5 electron-hole pairs in order to reduce electronic noise created in the detector cell circuitry 70.

For a typical circuit substrate detector material having 600-micron thickness something of the order of 10,000 electron-hole pairs are generated due to incident
10 high-energy radiation. However, this is reduced to around the order of less than 2000 electron-hole pairs when the circuit substrate material 380 is thinned to a thickness of around 100 microns. Therefore, thinned circuit substrate material advantageously reduces radiation-induced noise in detector cell circuits.

15 Additionally, the applicant has observed that if the substrate material is thinned then the capacitance 398 between the detector and the circuit substrate material is reduced, thereby leading to a faster transfer of charge from the detector to the detector cell circuitry.

20 The thinned circuit substrate wafer 420 is then etched in a Plasma Enhanced Reactive Ion Etch (PERIE) or Inductive Coupled Plasma (ICP) type etcher and the silicon etched through at respective detector cell contact regions corresponding to a circuit contact for the detector substrate circuitry. Typically, the detector circuitry is CMOS circuitry, but other circuitry may be used.

25 A process for fabricating an imaging device having detector cell contact pads electrically coupled to associated detector cell circuits will now be described with reference to Figure 16 of the drawings. Although only one detector contact pad and associated detector cell contact is illustrated, it will be evident to the person of
30 ordinary skill in the art that the process may be applied to an array of detector pads/cell contacts. Furthermore, the process may also be utilised to form conductive via holes such as illustrated in Figures 10 and 11.

Figure 16A illustrates a part of a CMOS detector circuit substrate 420 including a circuit contact pad 432. As shown in Figure 16B, photo-resist 432 is deposited over the CMOS detector circuit substrate, including the circuit contact pad 432. The photo-resist 432 is then exposed through a suitable photo-lithographic mask to leave an area of the circuit contact pad 432 uncovered as illustrated in Figure 16C. Typically, the photo-resist 432 is exposed to leave 30-micron holes over the circuit contact pads 432. A 30-micron hole would give a 5:1 aspect ratio for a through hole in a 150-micron thick detector circuit substrate. This should yield through holes having substantially clear, straight sidewalls. Evidently, other suitable dimensions for the hole diameter and substrate (wafer) thickness may be used. Additionally, the holes need not be circular, but may be oval, or have straight sides or be in the form of a square or rectangle for example.

The detector circuit substrate 420 is then etched through the exposed regions of the photo-resist 432, for example using a typical industry standard process such as a $\text{SF}_6/\text{O}_2/\text{HBr}$ type process, to produce through via hole 434 in the circuit substrate 420, as illustrated in Figure 16D. The photo resist will then be removed from the detector circuit substrate.

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The detector circuit substrate CMOS is attached to a detector substrate 1 such that the through holes 434 correspond to detector substrate contact pads 68. The CMOS detector circuit substrate 3 is attached to detector substrate 60 by any suitable adhesive material. For example, photo-resist 436 may be applied to one or other surface of the CMOS detector circuitry substrate 3 and detector substrate 60 which has sufficient adhesive properties to attach the respective substrates together. Optionally, an adhesive layer 438 may be applied to one or other of the substrate surfaces. If an adhesive layer 438 is used then the detector contact pad 68 are left uncovered. In the case of photo resist 436, the photo-resist may be applied across the whole of the surface of one or other substrate and then exposed once the substrates have been attached together in order to uncover detector contact pads 68.

A photo resist layer 440 is deposited over the circuit and detector substrate assembly. Subsequently, a mask is placed over photo resist 440, and the photo resist exposed to leave uncovered the region corresponding to the via hole 434, as illustrated in Figure 16F. In the next step, gold 442 is deposited over the substrate assembly as illustrated in Figure 15G. As can be seen in Figure 16G, gold is deposited on the detector contact pad 68 along the walls of the via hole 434 and onto circuit contact pad 432 thereby providing electrical coupling between circuit contact pad 432 and detector contact pad 68. Gold may be deposited via any suitable means. For example sputtering, electrical chemical deposition, E-Less, or Electro-Less or Electric-less chemical deposition.

Photo-resist 440 is subsequently removed, thereby removing the excess gold, as illustrated in Figure 16H to leave a CMOS detector circuit substrate 3 electrically coupled to a detector substrate 60 via a conductive through via hole 434. In the particular arrangement illustrated in Figure 16H the side walls of the through hole 434 are coated with conductive material. Evidently, more gold could be deposited in the step illustrated in Figure 16G to create a more solid in-fill of through via hole 434. However, such extra in-fill is not necessary and would lead to unnecessary expense.

As illustrated in Figure 17, by providing conductive via holes through the circuit substrate 362 imaging devices 320 may be placed end-to-end without any "dead spaces". The conductive via holes 322 may couple from the underside of the imaging device to the mount 4.

Figure 18 illustrates an arrangement, shown upside down relative to Figure 17, in which by placing the metal contacts on the underside of the CMOS circuit substrate 380 configured in accordance with Figures 14 and 15, the imaging device output signals may be wire bond coupled to amounting PCB 4. Other suitable bond connections may be made, for example ball-grid-arrays (BGA), conductive epoxy and stud-bumps. In this way, a totally flat detector surface may be built to any size comprising large flat panels without any need to tilt adjacent imaging devices as is necessary in prior art arrangements.

Figure 19 illustrates a radiation imaging cassette 500, incorporating imaging devices and imaging device tiles in accordance with embodiments of the present invention. The cassette 500 is made to be a plug-in replacement for conventional film
5 cassettes in imaging systems, and its dimensions are configured accordingly dependent on the system for which the cassette is to provide the plug-in replacement.

The cassette 500 has a housing 502 in which are supported a 3x3 array of imaging devices having a separate detector substrate 504 and CMOS circuit substrate
10 506. The CMOS circuit substrate 506 may be thinned in accordance with one embodiment of the invention. Each imaging device may be supported on a separate mount (not shown) to form an imaging device tile 508. The imaging device tiles 508 are mounted on an analogue printed circuit board (PCB) 510 in an edge-to-edge configuration thereby providing a flat mounted continuous large area imaging surface
15 512. Analogue PCB 510 preferably comprises at least all the analogue electronics for the imaging device tiles 508 supported thereon, including control, readout and power supply signals.

A side cut-out view is shown as detail 514, and illustrates how the imaging
20 devices may be placed edge-to-edge. The interface region 516 of each imaging device is shown having two rows of through via holes 518 extending from the upper layer 520 of the CMOS circuit substrate 506, to the lower layer 522.

The analogue PCB 510 is connected to a digital motherboard 524 by way of a
25 mother/daughter board connector 526. Input/output control, readout and power supply signals are also coupled to the analogue circuitry module by means of connector 526.

The digital motherboard 524 comprises the digital electronics for controlling
30 imaging acquisition and read-out and resetting of the imaging device tiles. Other circuitry, such as further analogue circuitry, may be disposed on circuit board 524. Digital motherboard has an input/output connector 528 for interfacing the imaging cassette 500 with the rest of an imaging system.

Referring now to Figure 20, there is schematically illustrated a radiation imaging system 530 including an imaging cassette 500 as described above.

5 An object 532, for example *in vivo* or *in vitro* human tissue, is irradiated with X-rays 534 from a source 536. The object 532 may be stationary or moving relative to imaging cassette 500. Image signals are readout from the imaging cassette 500 via I/O connector 528 over a high speed (e.g. video data rate) readout interface 538 to a host controller 540. Image processing is then carried out on computer system 542, having a display 542 for displaying the image.

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In view of the foregoing description of particular embodiments of the invention it will be appreciated by a person skilled in the art that various additions, modifications and alternatives thereto may be envisaged. For example, the detector cell circuits may utilise technology other than simple CMOS technology, including but not limited to TTL, CMOS+, bipolar and BiCMOS. Furthermore, the circuit substrate material need not be silicon, but may be any other suitable semi-conductor material. As will be appreciated from a reading of the foregoing descriptions of different types of image cell and detector cell circuitry, embodiments in accordance with the present invention may utilise many different types of image cell and detector cell circuitry, not limited to those described herein in detail. Other examples of detector cell circuitry includes, without limitation: energy discriminator circuitry; pulse shaping circuitry; pulse amplifying circuitry; analogue to digital converter circuitry; and rate divider circuitry.

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25 Although etching of a silicon circuit substrate has been described using a $\text{SF}_6/\text{O}_2/\text{HBr}$ type process, other suitable processes may be used for etching silicon, and as appropriate for substrates other than silicon.

In another aspect, the present invention provides a semiconductor circuit substrate, comprising:

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circuit means supported by said circuit substrate;

means for providing one or more conductive paths supported by said circuit substrate for supplying signals to and/or from said circuitry, said one or more conductive paths extending from said circuitry to an interface region of said circuit substrate; and

5 means for providing one or more signal pathways extending from said interface region through said circuit substrate to a surface of said substrate, said one or more signal pathways electrically coupled to said one or more conductive paths to provide an external signal interface for said circuitry.

10 In another aspect, the present invention provides a method for fabricating a semiconductor circuit substrate, the method comprising the steps for:

(a) etching one or more pathways through a semiconductor circuit substrate from a surface thereof at a location corresponding to an interface region of said circuit substrate, said one or more pathways corresponding to at least one of control signal, readout and power supply lines for supplying at least one of control signal, readout and power to a circuit in a layer of said circuit substrate; and

15 (b) depositing conductive material in said one or more pathways to provide one or more conductive pathways between said at least one of control signal, readout and power supply lines and a surface of said circuit substrate.

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The scope of the present disclosure includes any novel feature or combination of features disclosed therein either explicitly or implicitly or any generalisation thereof irrespective of whether or not it relates to the claimed invention or mitigates any or all of the problems addressed by the present invention. The applicant hereby gives notice that new claims may be formulated to such features during the prosecution of this application or of any such further application derived therefrom. In particular, with reference to the appended claims, features from dependent claims may be combined with those of the independent claims and features from respective independent claims may be combined in any appropriate manner and not merely in the specific combinations enumerated in the claims.

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CLAIMS

1. A semiconductor circuit substrate, comprising:
active circuitry supported by said circuit substrate;
5 one or more conductive paths supported by said circuit substrate for supplying at least one of control, readout and power supply signals to and/or from said active circuitry, said one or more conductive paths extending from said active circuitry to an interface region of said circuit substrate; and
one or more signal pathways extending from said interface region through said
10 circuit substrate to a surface of said substrate, said one or more signal pathways electrically coupled to said one or more conductive paths to provide an external signal interface for said active circuitry.
2. A semiconductor circuit substrate according to claim 1, said one or more signal
15 pathways comprising a low impedance conductive material.
3. A semiconductor circuit substrate according to claim 2, said one or more signal pathways comprising a via hole filled with said conductive material.
- 20 4. A semiconductor circuit substrate according to claim 2, said one or more signal pathways comprising a via hole having internal walls coated with said conductive material.
5. A semiconductor circuit substrate according to any one of claims 2 to 4, said
25 conductive material being a metallic material.
6. A semiconductor circuit substrate according to claim 5, said metallic material comprising a metal.
- 30 7. A semiconductor circuit substrate according to any preceding claim, comprising a reduced depth in said interface region relative to the rest of said substrate.

8. A semiconductor circuit substrate according to any preceding claim, said interface region including an edge of said substrate.
9. A semiconductor circuit substrate according to any preceding claim, further
5 comprising conductive shielding around a substantial part of said one or more signal pathways.
10. A semiconductor circuit substrate according to claim 9, said conductive shielding coupled to a reference potential.
- 10 11. A semiconductor circuit substrate according to any preceding claim, said circuitry formed in a surface region of said circuit substrate opposing said circuit substrate region to which said one or more signal pathways extend.
- 15 12. A semiconductor circuit substrate according to any preceding claim, said circuitry comprising radiation detection circuitry.
13. A semiconductor circuit substrate according to claim 12, said circuitry comprising a detector cell circuit configured to receive charge from a detector cell responsive to
20 incident radiation to generate charge.
14. A semiconductor circuit substrate according to claim 13, said detector cell circuit configured to receive charge from a detector cell disposed on a detector substrate separate from said circuit substrate.
- 25 15. A radiation detection device, comprising:
a semiconductor circuit substrate according to claim 13 or claim 14; and
a detector substrate including a detector cell responsive to incident radiation to
30 generate charge, said detector cell including at least one detector cell contact for coupling charge from said detector cell to said detector cell circuit.

16. A semiconductor circuit substrate according to claim 13 or 14, said circuitry comprising an array of detector cell circuits associated with a corresponding array of detector cells, each detector cell responsive to radiation incident thereon to generate charge, and wherein respective detector cell circuits of said array of detector cell
5 circuits are configured to receive charge from associated detector cells of said array of detector cells.

17. An imaging device for imaging radiation, comprising:
a semiconductor circuit substrate according to claim 16; and
10 a detector substrate including an array of detector cells each including a detector cell contact for coupling charge from said detector cell; wherein
respective detector cell circuits of said array of detector cell circuits are configured to receive charge from detector cell contacts of associated detector cells of said array of detector cells.

15 18. A semiconductor circuit substrate according to any one of claims 13 to 17, said detector cell circuit or circuits comprising one or more of the following:
charge accumulation circuitry; counter circuitry; read out circuitry; energy discriminator circuitry; pulse shaping circuitry; pulse amplifying circuitry; analogue to
20 digital converter circuitry; and rate divider circuitry.

19. A radiation detection device according to claim 16, wherein said detector substrate comprises a bias contact on a surface thereof opposing said detector cell contact, said bias contact defining said detector cell in co-operation with said detector cell contact .

25 20. A radiation imaging device according to claim 18, wherein said detector substrate comprises a bias contact on a surface opposing said detector cell contacts, said bias contact defining said array of detector cells in co-operation with said detector cell contacts.

30 21. A radiation detection device tile, comprising:
a radiation detection device according to claim 16 or claim 19; and

a mount for mounting said detection device;

said mount including contacts for conductively coupling said conductive signal pathways to corresponding external signal lines disposed on said mount.

5 22. A radiation imaging device tile, comprising:

a radiation imaging device according to claim 18 or claim 20; and

a mount for mounting said detection device;

said mount including contacts for conductively coupling said conductive signal pathways to corresponding external signal lines disposed on said mount.

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23. A method for fabricating a semiconductor circuit substrate, the method comprising the steps of:

(a) etching one or more signal pathways through a semiconductor circuit substrate from a surface thereof at a location corresponding to an interface region of said circuit
15 substrate, said one or more signal pathways corresponding to at least one of control signal, readout and power supply lines for supplying at least one of control signal, readout and power to an active circuit supported by said circuit substrate; and

(b) depositing low impedance conductive material in said one or more signal pathways to provide one or more low impedance conductive signal pathways between
20 said at least one of control signal, readout and power supply lines and a surface of said circuit substrate.

24. A method according to claim 23, step (a) further comprising the steps of:

(a)(i) depositing photo-resistive material over said circuit substrate;

25 (a)(ii) applying a photo-lithographic mask having one or more openings corresponding in said interface region;

(a)(iii) exposing said photo-resistive material through said openings in said mask;

(a)(iv) removing said exposed photo-resistive material to expose said circuit
substrate; and

30 (a)(v) etching said exposed circuit substrate to etch said one or more signal pathways through said substrate.

25. A method according to claim 23 or claim 24, wherein said etching forms one or more via holes for forming said one or more low impedance signal pathways.

26. A method according to claim 25, wherein step (b) further comprises filling said one or more via holes with low impedance conductive material.

27. A method according to claim 25, wherein step (b) further comprises coating internal walls of said one or more via holes with said low impedance conductive material.

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28. A method according to any one of claims 23 to 28, wherein said low impedance conductive material comprises a metallic material.

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29. A method according to claim 28, wherein said metallic material comprises a metal.

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30. A method according to any one of claims 23 or 29, further comprising prior to step (a), the step of reducing the thickness of said circuit substrate in said interface region relative to the rest of the substrate.

31. A method according to any one of claims 25 to 30, further comprising prior to step (b), the steps of:

(b)(i) depositing a conductive shielding over internal walls of said one or more via holes; and

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(b)(ii) depositing an insulating layer over said conductive shielding.

32. A method of fabricating a radiation detection device, comprising:

a method of fabricating a circuit substrate according to any one of claims 23 to 31;

and

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fabricating said circuit as a radiation detection circuit.

33. A method of fabricating a radiation detector device, comprising:

a method of fabricating a circuit substrate according to any one of claims 23 to 31;
and

further comprising fabricating said circuit to receive charge from a detector cell
formed in a detector substrate separate from said circuit substrate, said detector cell
5 responsive to incident radiation to generate charge.

34. A method of fabricating a radiation detector device, comprising:

a method according to claim 33; and

coupling a detector substrate, including a detector cell responsive to incident
10 radiation to generate charge, to said circuit substrate to form a conductive coupling for
providing said charge to said radiation detection circuit.

35. A method of fabricating an imaging device for imaging radiation, comprising:

a method of fabricating a circuit substrate according to any one of claims 23 to 31;
15 and

fabricating a plurality of said circuits to form an array of radiation detection
circuits.

36. A method according to claim 35, further comprising fabricating said array of
20 radiation detection circuits to receive charge from a corresponding array of detector
cells formed in a detector substrate separate from said circuit substrate, said detector
cells responsive to incident radiation to generate charge.

37. A method according to claim 36, further comprising coupling a detector substrate,
25 including said array of detector cells responsive to incident radiation to generate
charge, to said circuit substrate to form a conductive coupling for providing said
charge from respective detector cells to associated radiation detection circuits.

38. A method of forming a radiation detector device tile, comprising:

30 a method according to claim 33 or claim 34; and

coupling said radiation detector device to a mount, including conductively coupling said one or more signal pathways to corresponding external signal lines disposed on said mount.

5 39. A method of forming an imaging device tile, comprising:

a method according to claim 35 or 36; and

coupling said imaging device to a mount, including conductively coupling said one or more signal pathways to corresponding external signal lines disposed on said mount.

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40. A radiation imaging cassette, comprising:

a housing; and

a plurality of radiation imaging device tiles according to claim 22 mounted in said housing and arranged to form a large area imaging tiled array.

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41. A radiation imaging cassette according to claim 40, wherein said imaging device tiles are arranged to form a 3×3 array of imaging devices.

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42. A semiconductor detector circuit substrate substantially as hereinbefore described, and with reference to Figures 10 and 12 to 14, and Figures 11 and 12 to 14 respectively of the drawings.

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43. A radiation detection device substantially as hereinbefore described, and with reference to Figures 10 and 12 to 14, and Figures 11 and 12 to 14 respectively of the drawings.

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44. An imaging device for imaging radiation substantially as hereinbefore described, and with reference to Figures 10 and 12 to 14, and Figures 11 and 12 to 14 respectively of the drawings.

45. A radiation detection device tile substantially as hereinbefore described, and with reference to Figures 10 and 12 to 14, and Figures 11 and 12 to 14 respectively of the drawings.

5 46. A radiation imaging device tile substantially as hereinbefore described, and with reference to Figures 10 and 12 to 14, and Figures 11 and 12 to 14 respectively of the drawings.

47. A method for fabricating a semiconductor detector circuit substrate substantially as
10 hereinbefore described, and with reference to Figures 10 and 12 to 14, and Figures 11 and 12 to 14 respectively of the drawings.

48. A method of fabricating a radiation detection device substantially as hereinbefore described, and with reference to Figures 10 and 12 to 14, and Figures 11 and 12 to 14
15 respectively of the drawings.

49. A method of fabricating an imaging device substantially as hereinbefore described, and with reference to Figures 10 and 12 to 14, and Figures 11 and 12 to 14 respectively of the drawings.

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50. A method of forming a radiation detector device tile substantially as hereinbefore described, and with reference to Figures 10 and 12 to 14, and Figures 11 and 12 to 14 respectively of the drawings.

25 51. A method of forming an imaging device tile substantially as hereinbefore described, and with reference to Figures 10 and 12 to 14, and Figures 11 and 12 to 14 respectively of the drawings.

52. A method of forming an imaging cassette substantially as hereinbefore described,
30 and with reference to Figures 19 and 20 of the drawings.

ABSTRACTCIRCUIT SUBSTRATE AND METHOD

- 5 A semiconductor circuit substrate supporting active circuitry, and conductive paths for supplying control, readout and power supply signals to and/or from the active circuitry. The conductive paths extend from the active circuitry to an interface region of the circuit substrate. A plurality of signal pathways extend from the interface region through the circuit substrate to a surface of the substrate. The signal pathways are
- 10 electrically coupled to the conductive paths to provide an external signal interface for the circuitry from the substrate.

Fig. 10